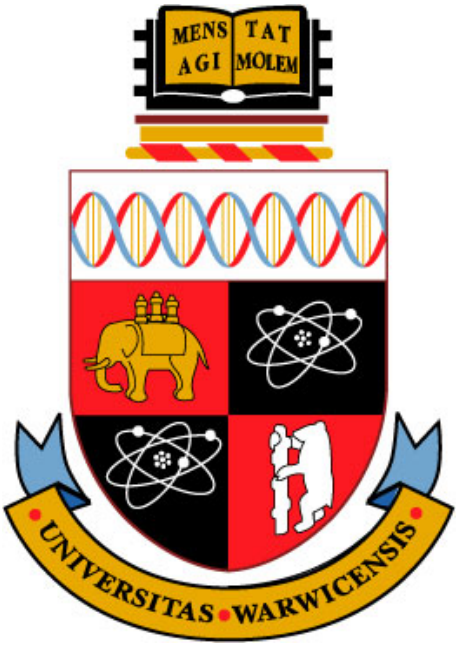
Development of 4H-SiC PiN Diodes for High Voltage Applications



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Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has not been submitted for a degree at any other University. Except where specifically stated, all of the work described in this thesis was carried out by the author or under his direction in the School of Engineering at the University of Warwick from October 2010 until February 2014.

C. A. Fisher
February 2014 (revised May 2014)

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Publications

Journal Publications

1. **C. A. Fisher**, M. R. Jennings, Y. K. Sharma D. P. Hamilton, S. M. Thomas, P. M. Gammon, A. Pérez-Tomás, S. E. Burrows and P. A. Mawby

   'Improved performance of 4H-SiC PiN diodes using a novel combined high temperature oxidation and annealing process'

   Manuscript accepted for publication (subject to revisions) in IEEE Transactions on Semiconductor Manufacturing, April 2014.

2. M. R. Jennings, **C. A. Fisher**, D. Walker, A. Sanchez, A. Pérez-Tomás, D. P. Hamilton, P. M. Gammon, S. E. Burrows, S. M. Thomas, Y. K. Sharma, F. Li and P. A. Mawby

   'Physical and electrical characterisation of 3C-SiC and 4H-SiC for power semiconductor device applications'

   Physics of Semiconductor Devices, pp. 929-932 (2014).

3. S. Jahdi, O. Alatise, **C. A. Fisher**, L. Ran and P. A. Mawby

   'An evaluation of silicon carbide unipolar technologies for electric vehicle drivetrains'

   Manuscript accepted for publication in IEEE Journal of Emerging and Selected Topics in Power Electronics, February 2014.

4. S. M. Thomas, Y. K. Sharma, M. A. Crouch, **C. A. Fisher**, M. R. Jennings and P. A. Mawby

   'Enhanced field effect mobility on 4H-SiC by oxidation at 1500°C'

   Manuscript accepted for publication (subject to revisions) in Solid-State Electronics, April 2014.

5. **C. A. Fisher**, M. R. Jennings, A. T. Bryant, A. Pérez-Tomás, P. M. Gammon, P. Godignon and P. A. Mawby

   'Physical modelling of 4H-SiC PiN diodes'

   Mat. Sci. Forum. 717-720, pp. 993-996 (2012).

6. M. R. Jennings, A. Pérez-Tomás, A. Bashir, A. M. Sanchez, A. Severino, P. J. Ward, S M. Thomas, **C. A. Fisher**, P. M. Gammon, M. Zabala, S. E. Burrows, B. T. Donnellan, D. P. Hamilton, D. Walker and P. A. Mawby

   'Bow free 4" diameter 3C-SiC epilayers formed upon wafer-bonded Si/SiC substrates'

   ECS Solid State Letters, 1(6), pp. 85 (2012).

Conference Publications

1. **C. A. Fisher**, M. R. Jennings, Y. K. Sharma, D. P. Hamilton, S. M. Thomas, P. M. Gammon, A. Pérez-Tomás, S. E. Burrows and P. A. Mawby

   'On the application of novel high temperature oxidation processes to enhance the performance of high voltage silicon carbide PiN diodes'

   Manuscript accepted for presentation at EPE '14-ECCE Europe, Finland, August 2014.

2. **C. A. Fisher**, M. R. Jennings, Y. K. Sharma, S. M. Thomas, F. Li, P. M. Gammon, D. P. Hamilton, A. Pérez-Tomás, S. E. Burrows and P. A. Mawby

   'On the application of a novel combined implant activation anneal / SiO_2 passivation process for 4H-SiC PiN diodes'

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3. **C. A. Fisher**, M. R. Jennings, Y. K. Sharma, D. P. Hamilton, S. M. Thomas, F. Li, P. M. Gammon, A. Pérez-Tomás, S. E. Burrows and P. A. Mawby

   'Enhanced forward bias operation of 4H-SiC PiN diodes using high temperature oxidation'

   Manuscript presented at the Materials Research Society (MRS), San Francisco, USA, April 2014.

4. M. R. Jennings, **C. A. Fisher**, D. Walker, A. Sanchez, A. Pérez-Tomás, D. P. Hamilton, P. M. Gammon, S. E. Burrows, S. M. Thomas, Y. K. Sharma, F. Li and P. A. Mawby

   'On the Ti_3SiC_2 metallic phase formation for robust p-type 4H-SiC ohmic contacts'

   Presented at the International Conference on Silicon Carbide and Related Materials (ICSCRM) 2013, Miyazaki, Japan, Sept. 29th - Oct. 4th.

5. P. M. Gammon, **C. A. Fisher**, V. A. Shah, M. R. Jennings, A. Pérez-Tomás, S. E. Burrows, M. Myronov, D. R. Leadley and P. A. Mawby

   'The cryogenic testing and characterisation of SiC PiN diodes'

   Presented at the International Conference on Silicon Carbide and Related Materials (ICSCRM) 2013, Miyazaki, Japan, Sept. 29th - Oct. 4th.

6. S. M. Thomas, M. R. Jennings, Y. K. Sharma, **C. A. Fisher** and P. A. Mawby

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Abstract

Despite the excellent electrical and thermal properties of 4H-silicon carbide (SiC), the fabrication of high-voltage SiC power devices is still proving problematic, being hindered by material defects resulting in low carrier lifetimes and forward voltage drift, and sub-optimum ohmic contacts to p-type material. The PiN diode is one such device that suffers from the aforementioned problems, though at the same time is sought after for high voltage power electronics applications due to the prospect of greatly reduced power losses and increased power handling capability than the Si devices currently in use. As such, this thesis is focussed on the development of these devices, investigating various device structures to achieve high reverse blocking voltages as well as developing novel fabrication processes to improve the electrical performance of the devices.

Electrical characterisation of ohmic contacts to p-type 4H-SiC showed that Ti/Al-based metal schemes offered the lowest specific contact resistivity of approximately 2.2×10^{-6} Ω-cm^2, which was achieved after annealing at 1000°C for 2 minutes. Physical analysis showed that these annealing conditions were optimum for formation of the Ti_3SiC_2 alloy at the metal-semiconductor interface, the presence of which was found to correlate with lower specific contact resistivity values. Electrical characterisation of first generation PiN diodes designed for blocking 3.3 kV showed that the fabricated devices had a differential on-resistance ($R_{on,diff}$) of 17 mΩ-cm^2 at 100 A/cm^2 and 25°C, and near-ideal ($\eta = 1.3$) characteristics in the diffusion current regime. Based on the measured reverse saturation currents, the carrier lifetime of the fabricated devices was estimated to be 480 ns. Reverse leakage currents were found to vary significantly across the devices, from 5 nA/cm^2 up to 200 μA/cm^2 at 100 V reverse bias and 25°C. Second generation 3.3 kV PiN diodes, which featured a B-implanted JTE structure, were found to block a maximum reverse voltage of 2.8 kV, which was around 85% of the target value.

PiN diodes fabricated with a drift region designed for blocking 10 kV underwent thermal oxidation processes at temperatures ranging from 1400°C to 1600°C in order to increase the carrier lifetime. Devices having undergone no lifetime enhancement treatment were found to have a $R_{on,diff}$ of 11.6 mΩ-cm^2 at 100 A/cm^2 and 25°C, and an ideality factor $\eta = 1.5$ in the diffusion current regime. PiN diodes that had undergone thermal oxidation were found to have improved forward characteristics, with devices oxidised at 1500°C exhibiting a $R_{on,diff}$ of around 9 mΩ-cm^2 at 100 A/cm^2 and 25°C, an improvement of nearly 25%. A novel combined thermal oxidation and annealing process was developed and applied to second generation 10 kV PiN diodes; a mean $R_{on,diff}$ of 4.45 mΩ-cm^2 was achieved, and a carrier lifetime of 1.21 μs was extracted from reverse recovery characteristics; these were both significant improvements on both the second generation control sample and the first generation thermally oxidised PiN diodes.

List of Abbreviations and Symbols

AC	Alternating Current
AFM	Atomic force microscopy
BJT	Bipolar junction transistor
BPD	Basal plane dislocation
CMP	Chemical mechanical polishing
CRT	Cathode ray tube
CSC	Current source converter
DC	Direct Current
DFT	Density functional theory
DLTS	Deep level transient spectroscopy
DUV	Deep ultra-violet
EDAX	Energy dispersive X-ray analysis
FE	Field emission
FEG	Field-emission gun
GTO	Gate turn-off thyristor
HTCVD	High temperature chemical vapour deposition
HVDC	High Voltage Direct Current
ICP	Inductively coupled plasma
IGBT	Insulated gate bipolar transistor
IGSF	In-grown stacking fault
JFET	Junction field-effect transistor
JTE	Junction termination extension
LAGB	Low-angle grain boundary
LCC	Line-commutated conversion
LED	Light-emitting diode
MLC	Multi-level converter
MOSFET	Metal-oxide-semiconductor field-effect transistor
MZ-JTE	Multiple-zone JTE
NPT	Non punch-through

PT	Punch-through
PVT	Physical vapour transport
PWM	Pulse width modulation
R-G	Recombination-Generation
RAF	Repeated *a*-face
RIE	Reactive ion etching
RTA	Rapid thermal annealing
SBD	Schottky barrier diode
SCC	Self-commutated conversion
SCR	Silicon controlled rectifier
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectrometry
SJ	Super junction
SM-JTE	Space-modulated JTE
SRH	Shockley-Read-Hall
SRIM	Stopping and range of ions in matter
SZ-JTE	Single-zone JTE
TED	Threading edge dislocation
TEM	Transmission electron microscopy
TFE	Thermionic field emission
TLM	Transfer length method
TRPL	Time resolved photoluminescence
TSD	Threading screw dislocation
VSC	Voltage source converter
XRD	X-ray diffraction

Ag	Silver
Al	Aluminium
AlN	Aluminium nitride
Ar	Argon
Au	Gold
B	Boron
BOE	Buffered oxide etch
C	Diamond
CF_4	Tetrafluoromethane
GaN	Gallium nitride
Ge	Germanium
HCl	Hydrochloric acid
HF	Hydrofluoric acid
HNO_3	Nitric acid

K	Potassium
KOH	Potassium hydroxide
Na	Sodium
NaOH	Sodium hydroxide
Ni	Nickel
NiV	Nickel vanadium
NO	Nitric oxide
O_2	Oxygen
P	Phosphorous
SF_6	Sulphur hexafluoride
SiO_2	Silicon dioxide
TEOS	Tetraethyl orthosilicate
Ti	Titanium

$\mathscr{E}$	Electric field (V/cm)
$\mathscr{E}_C$	Critical electric field (V-cm)
$\mathscr{E}_{C,PP}$	Critical electric field of parallel-plane junction (V/cm)
A	Area (cm^2)
A^*	Richardson constant (A/cm^2-K^2)
B	Mobility asymmetry factor
BV_{PP}	Breakdown voltage of parallel-plane junction (V)
BV_{PT}	Breakdown voltage of a punch-through PiN diode (V)
C_{GC}	Gate-collector capacitance (F)
C_{GE}	Gate-emitter capacitance (F)
d	Half of drift region width (cm)
D_a	Ambipolar diffusion constant
D_n	Electron diffusion constant
D_p	Hole diffusion constant
D_{it}	Interface trap density (cm^{-2})
E_C	Bottom edge of conduction band (eV)
E_G	Band gap energy (eV)
E_i	Intrinsic Fermi level (eV)
E_V	Top edge of valence band (eV)
E_{00}	Characteristic energy (eV)
E_{Cn}	Conduction band energy in n-type material (eV)
E_{Cp}	Conduction band energy in p-type material (eV)
E_{Fn}	Quasi-Fermi level for n-type material (eV)
E_{Fp}	Quasi-Fermi level for p-type material (eV)
E_{Vn}	Valence band energy in n-type material (eV)
E_{Vp}	Valence band energy in p-type material (eV)

f_{SW}	Switching frequency (Hz)
h	Planck constant (J-s)
I_C	IGBT collector current (A)
I_F	Diode forward current (A)
I_G	Gate current (A)
I_{RP}	Diode peak reverse current (A)
J_0	Reverse saturation current density (A/cm^2)
J_F	Forward current density (A/cm^2)
J_G	Generation leakage current density (A/cm^2)
J_n	Electron current density (A/cm^2)
J_p	Hole current density (A/cm^2)
$J_{0,rec}$	Saturation recombination current density (A/cm^2)
J_{Diff}	Diffusion current density (A/cm^2)
J_{ns}	Saturation current density in $P+$ emitter (A/cm^2)
J_{ps}	Saturation current density in $N+$ emitter (A/cm^2)
J_{RP}	Peak reverse current density (A/cm^2)
Jn_{P+}	Electron current density in $P+$ emitter (A/cm^2)
Jp_{N+}	Hole current density in $N+$ emitter (A/cm^2)
k	Boltzmann constant (J/K)
L	Inductance (H)
L_a	Ambipolar diffusion length (cm)
L_n	Electron diffusion length (cm)
L_p	Hole diffusion length (cm)
L_T	Transfer length (cm)
m	Electron mass (Kg)
m^*	Hole effective mass
n	Free electron concentration (cm^{-3})
N_A	Doping concentration (p-type) (cm^{-3})
N_A^+	Ionised dopant concentration (p-type) (cm^{-3})
N_D	Doping concentration (n-type) (cm^{-3})
N_D^+	Ionised dopant concentration (n-type) (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
n_n	Electron concentration in n-type material (cm^{-3})
n_p	Electron concentration in p-type material (cm^{-3})
N_t	Defect concentration (cm^{-3})
n_{n0}	Electron concentration in n-type semiconductor in equilibrium (cm^{-3})
n_{p0}	Electron concentration in p-type material in equilibrium (cm^{-3})
P	Perimeter (cm)
p	Free hole concentration (cm^{-3})
p_n	Hole concentration in n-type material (cm^{-3})
p_p	Hole concentration in p-type material (cm^{-3})

p_{0N+}	Equilibrium minority carrier concentration (holes) (cm^{-3})
$P_{D,rr}$	Power dissipation during reverse recovery (W)
p_{n0}	Hole concentration in n-type semiconductor in equilibrium (cm^{-3})
p_{p0}	Hole concentration in p-type material in equilibrium (cm^{-3})
q	Electronic charge (C)
Q_{OPT}	Optimum JTE charge (C)
Q_{ox}	Fixed oxide charge (C)
Q_{rr}	Reverse recovery charge (C)
r	Radius (cm)
R_C	Contact resistance (Ω)
R_D	Drift region resistance (Ω)
r_d	Radius of curvature of the depletion layer boundary (cm)
r_J	Radius of curvature of the metallurgical junction (cm)
R_T	Total contact resistance between two adjacent contacts (Ω)
$R_{DS(on)}$	Specific on-resistance of a MOSFET (Ω-cm^2)
$R_{on,diff}$	Differential on resistance (Ω-cm^2)
R_{sh}	Sheet resistance ($\Omega/\square$)
S	Surface recombination / generation velocity (cm/s)
s_P	Surface recombination velocity along mesa perimeter of a PiN diode (cm/s)
T	Temperature (K)
T_L	Lattice temperature (K)
t_{ox}	Oxide thickness (cm)
t_{rr}	Reverse recovery time (s)
V_a	Applied voltage (V)
V_F	Forward voltage drop of overall PiN diode (V)
V_M	Forward voltage drop of modulated PiN diode drift region (V)
V_R	Reverse clamping voltage (V)
V_{AK}	Diode voltage (V)
V_{bi}	Diode built-in voltage (V)
V_{CE}	IGBT collector-emitter voltage (V)
V_{GE}	IGBT gate-emitter voltage (V)
V_{N+}	Voltage drop of $N+$ emitter in a PiN diode (V)
V_{P+}	Voltage drop of $P+$ emitter in a PiN diode (V)
V_{TH}	Gate threshold voltage (V)
W_D	Width of drift region (cm)
W_d	Width of depletion region (cm)
W_R	Field ring width (cm)
W_S	Lateral depletion region width (cm)
W_{JTE}	Width of JTE region (cm)
W_{N+}	Depletion width in $N+$ emitter (cm)
W_{P+}	Depletion width in $P+$ emitter (cm)

W_{PP}	Depletion width of parallel-plane junction (cm)
α_n	Impact ionisation rate in n-type material (s^{-1})
α_p	Impact ionisation rate in p-type material (s^{-1})
γ	Emitter injection efficiency
γ_3	Auger recombination coefficient
λ	Thermal conductivity (W/cm-K)
λ_e	Electron wavelength (cm)
μ_g	Geometric mean
μ_n	Electron mobility (cm^2/V-s)
μ_p	Hole mobility (cm^2/V-s)
μ_{inv}	Inverted channel mobility (cm^2/V-s)
Φ_B	Schottky barrier height (eV)
ρ_C	Specific contact resistance (Ω-cm^2)
σ_g	Geometric standard deviation
σ_{n0}	Defect capture cross section for electrons (cm^2)
σ_{p0}	Defect capture cross section for holes (cm^2)
τ_{Auger}	Auger recombination-governed carrier lifetime (s)
τ_{eff}	Effective carrier lifetime in the PiN diode drift region (s)
τ_{HL}	High-level injection carrier lifetime (s)
τ_{n0}	Shockley-Read-Hall lifetime for electrons (s)
τ_{p0}	Shockley-Read-Hall lifetime for holes (s)
τ_{Rad}	Radiative recombination lifetime (s)
τ_{SC}	Carrier generation lifetime in depletion region (s)
τ_{SRH}	Shockley-Read-Hall lifetime (s)
υ_d	Carrier drift velocity (cm/s)
υ_{sat}	Carrier saturation velocity (cm/s)
υ_{th}	Carrier thermal velocity (cm/s)
ε_0	Vacuum permittivity (F/m)
ε_r	Dielectric constant
ε_S	Static dielectric constant of a semiconductor
ε_{Ox}	Static dielectric constant of SiO_2
ε_{SiC}	Static dielectric constant of 4H-SiC

Chapter

1 Introduction

Back in the late 19th century a war was being fought; one whose outcome has had a direct bearing on how electric power would be distributed during the decades thereafter. This war, referred to as the "War of the Currents", was fought between two principle adversaries. The first of these was Thomas Edison, who promoted the use of direct current (DC) for electric power distribution, and the second was George Westinghouse, who advocated the use of alternating current (AC). Although DC transmission was the standard for the United States during the initial years of electricity distribution (due to its compatibility with incandescent lamps, motors and storage batteries, as well as the ease of paralleling DC generators), its fundamental limitation of having a large voltage drop (relative to the transmission voltage) due to the resistance of the system conductors was glaringly apparent.

At the time, the only ways of overcoming this limitation of DC transmission were to generate power in close proximity to where it would be consumed, and install larger conductors as the demand for electricity increased. However, not only was this impractical, but it was also a costly solution due to the need for local power stations and vast

amounts of very thick copper wire. Furthermore, the fact that at this time DC could not easily be converted to higher or lower voltages meant that separate electrical lines had to be installed in order to supply power to appliances using different voltages, further exacerbating the costs involved with implementing the system, as well as introducing unnecessary hazards.

The use of an AC system, whereby transformers are used between a high voltage distribution system and the low voltage loads, allowed efficient power transmission to be realised without the limitations of the DC system. The benefits of AC transmission systems were obvious: fewer, larger generating plants could serve the load in a given area, and different sized loads could be served by the same distribution network simply by using a transformer with a suitable secondary voltage. Coupled with the introduction of a system for AC generators, transformers, motors, wires and lights towards the end of 1887, the AC system was deemed to be the future of electric power distribution. Though not without its own limitations, the huge advantage of simple stepping up and down of voltages ensured that AC transmission dominated over the subsequent decades.

Despite the dominance of AC transmission, work on developing a DC technology persisted. If conversion switches that were capable of withstanding high voltages could be developed, DC power transmission could succeed and be more efficient than AC transmission. In the early 20th century, electromechanical components were used to convert DC voltage levels, though these were commercially unsuccessful due to them requiring high maintenance and exhibiting high energy losses. The next-generation of DC transmission systems made use of grid-controlled mercury arc valves, and, in 1954, the first fully commercial static plant for high-voltage direct current (HVDC) transmission in the world went into service using this technology. It was this system that heralded the beginning of the modern era of HVDC transmission.

Since the advent of this first commercial system, power transmission systems have seen dramatic developments. The continued development of power solid-state devices for HVDC systems in the 1960s led to a rapid demise in the use of mercury arc valves due to the superior reliability that they offered, and acted as a catalyst for the provision of greater flexibility in grid-level transmission. Silicon solid-state technology has continued to develop in the decades since then, thus facilitating even greater grid flexibility. However, as a result of increasing electricity demand, projected to increase globally by 56% between 2010 and 2040 [1], combined with decreasing fossil fuel reserves, we are now at the crucial stage where we need to drastically transform our power grid if it is to remain reliable and secure for future generations.

Of paramount importance to this transformation of the power grid is the incorporation of HVDC transmission systems, which facilitate the connection of renewable energy sources to the grid, as well as enabling efficient bulk power transmission over long distances. However, the feasibility of HVDC systems depends heavily on the performance of the power electronics required to convert voltage levels. In addition to efficiency, cost and reliability are also crucial. Though silicon power electronics technology has seen vast improvements in each of these three areas in recent years, it seems that any further significant efficiency and performance gains are unlikely to be made using this semiconductor material. Furthermore, as transmission voltages increase, either the voltage rating of individual valves in a converter needs to increase, or the number of valves needs to increase. From a cost and reliability point of view, increasing the number of valves used in a converter is not the ideal solution.

With silicon power devices at their practical limit in terms of voltage rating and power handling, research has shifted towards looking at utilising so-called "wide band gap" semiconductor materials, whose properties are more suited for demanding high power

applications. Of the several wide band gap materials that are the subject of intensive research all around the globe, one material in particular is deemed to hold great promise for these high voltage, high power applications. This material is silicon carbide.

1.1 Background

The aim of this thesis is to design, fabricate and characterise 4H-silicon carbide (SiC) power rectifier diodes for high voltage applications, with a particular focus on optimising device performance using novel high temperature processing techniques. Also of key interest is the characterisation of dynamic (switching) behaviour of these devices at high voltages, and the impact they have on the performance of power electronics circuits.

The initial stimulus with regard to the design and fabrication of 4H-SiC power rectifier diodes was to build on previous work carried out at the University of Warwick [2] on the development of 4H-SiC power devices. Of particular interest was the realisation of bipolar devices in 4H-SiC due to their current development immaturity and the potential for their application in high voltage power transmission systems in the future. Work on one of the key issues in bipolar device processing, namely the formation of ohmic contacts to p-type 4H-SiC, had already took place at the University of Warwick [3]. The results of this work at the time were the best achieved within the research community, and, even today, have not been surpassed. As such, it seemed logical to further develop these findings and incorporate them into this next-generation of 4H-SiC power devices.

In addition to the above, the introduction of a new, state-of-the-art high temperature thermal oxidation furnace in the Science City cleanroom facility at Warwick, intended specifically for SiC device processing, has provided motivation for further research into high temperature fabrication processes for SiC devices. In the context of fabricating high

voltage rectifier diodes, the capability to perform high temperature oxidations is of great interest as it can be applied to increase the carrier lifetime in the semiconductor material by 'repairing' carbon-related defects, as demonstrated by Hiyoshi and Kimoto [4]. This repairing of defects occurs due to the removal of excess carbon atoms at the oxidising surface, which diffuse into the bulk of the semiconductor and end up residing on the previously vacant carbon sites. Due to equipment limitations, the work by Hiyoshi and Kimoto only investigated thermal oxidation up to 1400°C, though, encouragingly, this was found to be considerably more effective at increasing the carrier lifetime in the material for a given oxidation time. The capabilities at Warwick facilitate investigation of thermal oxides grown at temperatures well in excess of this (up to 1600°C), with the aim of further improving the extent to which the carrier lifetime can be enhanced in high voltage 4H-SiC power devices.

1.2 Motivation

As mentioned previously in this Chapter, power networks across the globe are in dire need of transformation if they are to continue to supply the ever-increasing quantities of power to society. A key part of this transformation is the increased use of renewable energy sources, such as wind and solar. HVDC systems are also required, for both long distance bulk power transmission as well as providing cross-country sub-marine transmission and connecting to offshore wind farms. Finally, the various conversion stages within the overall power network need to be made more energy efficient. All of these aspects of the power network are reliant on power electronics. 4H-SiC is widely considered to be the semiconductor material to replace silicon for high voltage power electronics, however, there are still technical problems that need to be resolved before 4H-SiC power devices

can be successfully applied in these demanding applications. The research presented in this thesis intends to further advance 4H-SiC high voltage power electronics technology to meet the aforementioned needs of the future power network.

1.3 Thesis Outline

The following Chapter first introduces the application space for the power devices being developed in this work, and presents some of the power electronics systems that these devices are intended to be used in. A discussion of the types of devices that are relevant to these power electronics systems is given, before moving on to how 4H-SiC can offer performance benefits over existing technologies as well as enabling power transmission systems of previously unachievable scale. In addition to the material advantages of 4H-SiC, its disadvantages are also discussed here. This Chapter concludes with a discussion of the current status of commercial SiC devices.

Chapter 3 presents some of the concepts that are key to the operation of high voltage 4H-SiC power diodes. The physical behaviour of these devices in the three principle operating states, namely the on-state, switching and reverse blocking, is analysed; this is then followed by a discussion of junction termination techniques, a crucial aspect of high voltage device design, and also carrier lifetime enhancement, again, an important aspect of high voltage bipolar devices. This Chapter next deals with the key fabrication issues that are prevalent for 4H-SiC power devices, then, finally, a review of the current state-of-the-art in high voltage 4H-SiC PiN diode technology is given.

In Chapter 4, the design and simulation of high voltage 4H-SiC PiN diodes is presented. Firstly, the physical models that are employed in numerical simulations are discussed. Following this, the designs of the device structures are outlined, and the results of numerical

simulations are presented. Chapter 5 outlines the characterisation techniques that have employed when evaluating the performance of the 4H-SiC PiN diodes that are fabricated in the subsequent Chapters. Physical, as well as electrical, characterisation methods are presented here.

Chapter 6 is the first experimental results Chapter, in which the results of fabrication process optimisation are presented. This Chapter deals with two key fabrication processes for 4H-SiC devices. Firstly, a study into material etching processes is presented. This is followed by a comprehensive study into the formation of ohmic contacts to p-type 4H-SiC, which has involved both physical and electrical characterisation to gain an understanding of the mechanisms behind the formation of low-resistance ohmic contacts.

The findings of Chapter 6 are then applied in Chapter 7, in which the development of PiN diodes targeting a blocking voltage of 3.3 kV is presented. This development work is presented in chronological order, charting the evolution of the devices with the aim of improving their electrical performance. Similarly, Chapter 8 presents the development work undertaken for PiN diodes targeting a higher blocking voltage of 10 kV, incorporating additional fabrication techniques specific to these higher voltage devices. Finally, Chapter 9 presents the conclusions of this thesis, as well as outlining suggestions for further work.

Chapter

2 Power Electronics and Silicon Carbide

Power electronics refers to the processing of electrical energy by means of semiconductor switching devices, as opposed to traditional electronics, which alludes to the processing of electrical information. Power electronics is a broad field, spanning a huge range of applications, from switch-mode power supplies in portable electronics products rated at several watts, through to converters for HVDC transmission systems that are rated up to several gigawatts. This applications space, and the power electronics devices associated with these applications, are illustrated in Figure 2.1. However, the scope of work in this thesis is limited to power transmission and distribution applications, i.e. 100 kVA and above, and, as such, the following discussion will be in the context of this particular application field.

In this Chapter, the power grid is first discussed, in order to provide the relevant background information for this work, as well as outlining the expected future trends of the grid. Next, the power electronics circuits that are required within the power grid are discussed, along with the semiconductor devices that are used in these circuits. Following this, the chapter moves to the subject of the wide band gap material silicon

carbide (SiC). The fundamental properties of SiC are discussed, to illustrate its advantages offered over other semiconductor materials. In addition, some of its shortcomings and the corresponding material challenges still being faced by researchers are presented. Finally, a review of the current status of SiC power devices is undertaken.

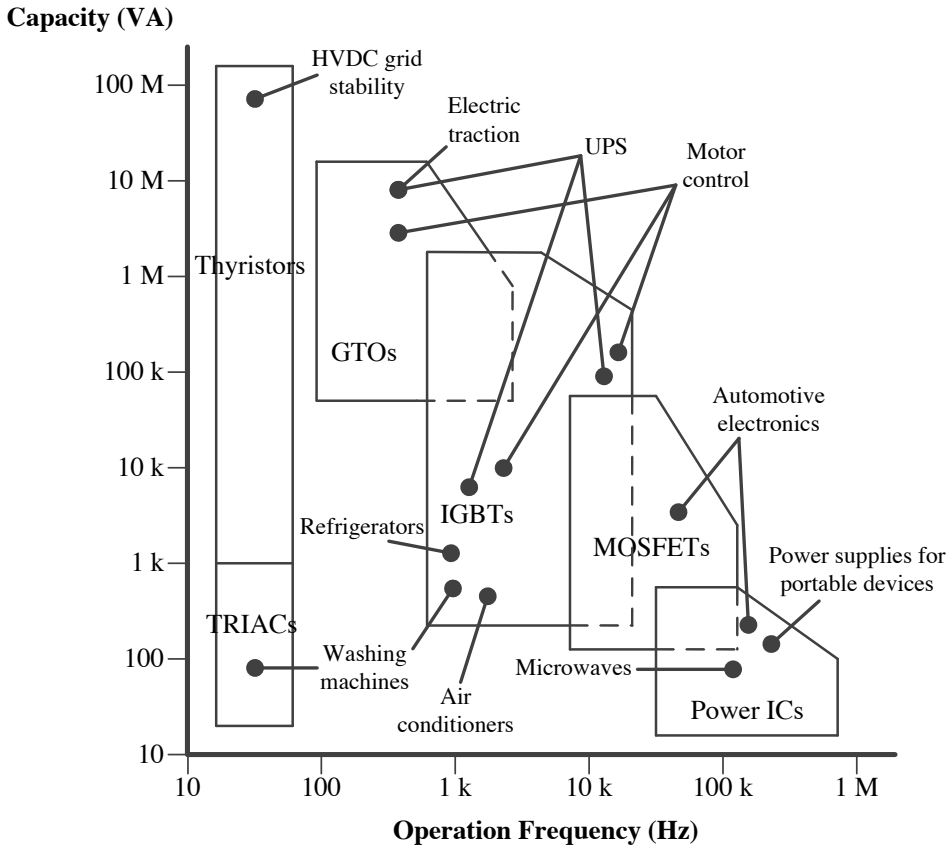


Figure 2.1: Applications of power electronics.

2.1 The Power Grid

The conventional power grid typically consists of three separate parts: generation, transmission and distribution, and can be considered a one-way power flow towards the end-

user. The generators, which are typically large units installed in strategic locations for operation with respect to the grid, are designed so as to produce relatively low voltages; as such, the generated power undergoes a series of voltage transformations to increase the voltage for efficient power transmission. The transmission system, which can be considered the backbone of the entire power system, allows power to be transferred from the large generation plants to large consumption centres as well as other sub-transmission and distribution systems. At the distribution end, the voltage is stepped back down to lower voltages, for economic and safe power distribution to the end user, who is conventionally considered as being a passive customer and does not contribute to the management of the system in any way. In this Section, each of these subcomponents of the power grid are discussed.

2.1.1 Power Generation

For many years, the conventional power grid has predominantly relied on the burning of CO_2 emitting fossil fuels for power generation, and continues to do so. However, with a diminishing fossil fuel supply, not to mention the drive to drastically reduce global CO_2 emissions as outlined in the Kyoto Protocol [5], it has become crucial that we look at employing other resources for our electricity needs. Moreover, as the global population is forecast to increase by around 25% between now and 2050 [6], it is logical to expect that the level of our electricity demand will also increase. This problem is further compounded by the increasing electrification in society - as an example, global sales of electric cars are set to increase from around 2 million units in 2013 to around 10 million units in 2022 [7]. As a result, it is not hard to see why our electricity grid is in desperate need of transformation if it is to be compatible with a low carbon economy as well as being

reliable and secure in the coming decades.

For the replacement of fossil fuel power generation, renewable energy sources such as wind, solar, wave and hydro are the most feasible options available to us. Nuclear fusion is still a distant prospect, thus these previously mentioned sources of energy are currently the only truly 'clean' forms of power generation. Encouragingly, many renewable energy technologies today are well developed, reliable and cost competitive when compared to conventional fuel generators. Furthermore, the cost of renewable energy technologies is on a falling trend and is expected to fall even further as demand for the technology and production levels increase. However, the successful large-scale integration of renewable energy sources into the power grid is heavily dependent on power electronics, as will be discussed in the subsequent Sections.

2.1.2 Power Transmission

As outlined in Chapter 1, the fundamental choice to make when considering a power transmission installation is whether to employ AC or DC transmission. This decision is based on an evaluation of transmission costs, technical considerations, and the reliability/availability offered by the two alternatives. The overall cost of a transmission line is comprised of two components: the capital investment required for the actual infrastructure, and costs incurred for operational requirements (i.e. losses). For similar voltage insulation requirements, a DC line with two conductors has the same power capacity as an AC line with three conductors of the same size. This means that, for a given power level, a DC line requires smaller, simpler and cheaper infrastructure, and has reduced conductor and insulator costs. Regarding the operational costs incurred, since there are only two conductors in a DC line compared to three in an equivalent capacity AC line, the

DC power transmission losses are reduced to approximately two-thirds of the comparable AC system [8]. Furthermore, the absence of skin effect in DC lines also marginally reduces the power losses compared to AC lines, and, lastly, dielectric losses are significantly lower for DC transmission.

On the other hand, the cost for DC transmission terminals is significantly higher than that for AC transmission terminals, due to the additional electrical components required for voltage conversion. As such, it is typically the case that AC transmission is more economical for short distances, but is more expensive for long transmission distances. This is illustrated in Figure 2.2. It can be seen that there is a "break-even distance" that signifies the point at which DC transmission becomes the most economical option. For overhead lines, the break-even distance can vary from about 500 to 800 km depending on the per unit line costs, whereas for a cable system the break-even distance is significantly lower, approaching 50 km [8].

When considering the technical aspects of the transmission system, it becomes apparent that DC transmission offers several advantages over AC transmission [8]. Firstly, the power carrying ability of DC lines is unaffected by the transmission distance. This isn't the case for AC lines, the power carrying ability of whom is inversely proportional to transmission distance due to power transfer limitations imposed by steady state and transient stability. Secondly, whilst in an AC system reactive power control is required to maintain a constant voltage at both ends of the line as the line loading is increased, DC lines have no such requirement. Thirdly, in order to overcome the problems of line charging and stability limitations, line compensation is required for AC lines. Again, DC lines have no such requirement. Fourthly, AC lines are constrained in that the interconnection of two AC power systems requires that the line power and frequency of the two systems is matched. However, even if the two systems are matched, problems such as large power

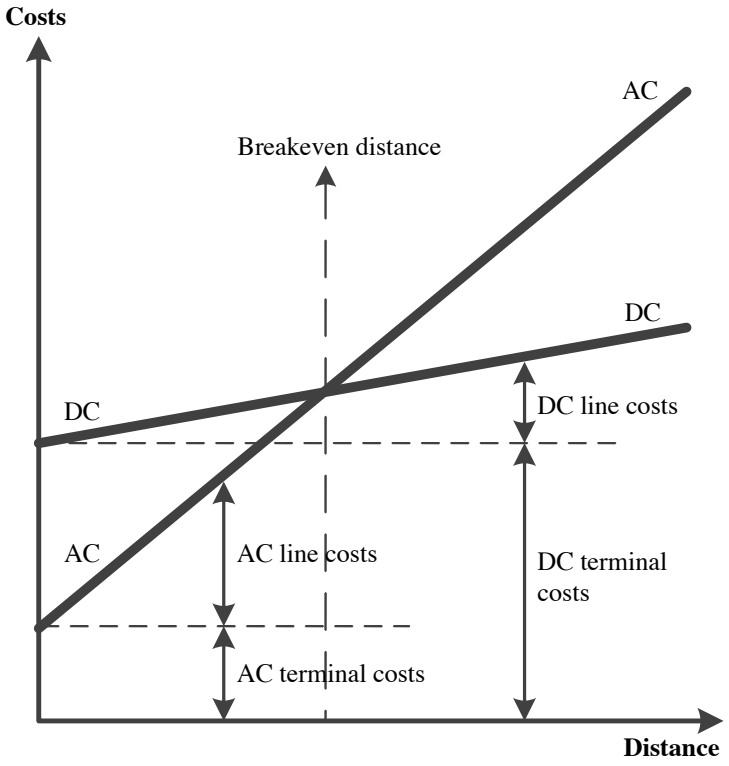


Figure 2.2: Comparison of AC and DC transmission system costs (taken from [8]).

oscillations, fault level increases and disturbance propagation between the two systems can occur. Due to the fast controllability of power flow in DC lines, these problems are eliminated in DC transmission systems. Lastly, the issue of ground impedance, which is present for AC transmission but is negligible for DC transmission, means that a DC link can operate for extended periods using just one conductor with ground return; this is not feasible for AC transmission.

Though the advantages of DC transmission are numerous, there are several problems which limits its application for power transmission:

1. Expensive conversion equipment.

2. Inability to use transformers to step voltages up/down.

3. Generation of harmonics (due to the approximated DC voltage obtained from the multi-phase converter).
4. Requirement of reactive power (for converter stations as opposed to transmission lines).
5. Complex control system requirements.

However, significant work in the field of DC transmission has led to technological advances aimed at overcoming the problems outlined above (with the exception of point 2). These are:

1. Increase in the voltage/current ratings of thyristor cells.
2. Modular construction of thyristor valves.
3. Twelve-pulse converter operation, meaning reduced harmonics.
4. Use of force-commutation.
5. Application of digital electronics and fibre optics in the control of converters.

As a result of these technological advances, the reliability of DC systems has improved while at the same time conversion costs have decreased. That said, costs still remain relatively high; as such, HVDC systems are typically restricted to specialist applications such as underground or underwater cables, long distance bulk transmission, asynchronous connection of AC systems and stabilisation of power flows in interconnected power systems [8]. In addition, the use of conventional thyristor cells in the widely-used line-commutated conversion (LCC) configuration restricts the flexibility of HVDC systems, due to the lack of turn-off controllability. This results in poor power factors and considerable waveform distortion, thus necessitating the use of complex and expensive reactive power compensation

and filtering. However, the shortcomings of LCC can be eliminated by employing the self-commutated conversion (SCC) technique, which utilises more advanced power electronics devices with turn-on and turn-off capability. The role of power electronics in the power grid is discussed in Section 2.2.

2.1.3 Power Distribution and the End-User

The final stage of the delivery of electricity to the end-user is the power distribution network. This network typically consists of medium-voltage power lines in the range 1 kV to 75 kV [9], substations and pole-mounted transformers, and low-voltage (sub-1 kV) distribution cabling, terminating at the electricity metering system of the end user. The voltage levels used in distribution systems and their topologies vary from country to country, and also from rural to urban areas. Due to the higher mains voltage used in Europe when compared, for example, to the United States (230 V and 120 V respectively), low-voltage substations typically supply a greater number of end users in Europe, as power can be distributed over a greater distance with acceptably low power loss. In addition, rural distribution systems typically use higher voltages than urban systems, due to the greater distances covered by distribution power lines. As inferred previously, the conventional power distribution system can be considered a 'one-way system', with power distributed to the end-user but with no facility for power to be fed from the end-user and back into the grid. This approach forms part of the concept of the "SmartGrid", discussed in the next Section.

2.1.4 The "SmartGrid" Concept

Though over the past few decades the development of power systems has been fairly slow, recent years have witnessed much more significant changes to these systems. These changes have occurred as a result of numerous factors, including the need for large-scale integration of renewable energy sources, existing ageing assets, energy efficiency requirements and increasing concern regarding the security of these systems. So that security, economy and efficiency demands are met whilst the operation of the power system continues to increase in complexity, a concept, referred to as the "SmartGrid", has emerged. Though there are many different views of the SmartGrid concept, a detailed definition is given by the US Department of Energy, which defines the SmartGrid as "self healing, enables active participation of consumers, operates resiliently against attack and natural disasters, accommodates all generation and storage options, enables introduction of new products, services and markets, optimises asset utilisation and operates efficiently, provides power quality for the digital economy" [10].

Central to the idea of the SmartGrid is the introduction of more advanced information and communication technologies (ICTs), thus adding more intelligence to the power grid. This has been made possible by recent developments of ICTs at acceptable costs, which, only a few years ago, were not possible. This integration of ICTs spans the entire hierarchy of the power grid, from smart metering systems at the end-user level, to systems used to control and optimise the power flow in HVDC connections. As illustrated in Figure 2.3, in contrast to the conventional power grid system, the SmartGrid features significant differences at the distribution and end-user levels. Though some renewable energy units, such as large offshore wind farms, will be connected directly at the top-end transmission level, the incentives of utilising renewable energy sources mean that smaller

and medium-sized units will be integrated into distribution level systems. However, due to the typically intermittent nature of energy sources such as wind and solar, and the fact that the conventional distribution systems have not been designed to integrate a significant number of generation units, it is crucial that intelligent management is incorporated at this system level.

Significant changes are also underway in the once passive end-user segment, which, conventionally, has not interacted dynamically with the power grid. Most notable is the emergence of the previously mentioned smart meter, which wirelessly communicates power usage and requirement data to the energy supplier, therefore regulating power with up-to-the-minute demand. It is envisaged that, in time, the smart meter will create the ability for electrical devices in the home to optimise their use based on a set of criteria, and will also allow consumers to not only access usage information remotely, but also control devices remotely; for example, to turn the heating on before the normal set time because they are returning home early. Furthermore, the smart meter will also monitor and control any electricity that consumers generate themselves, for example, by means of solar panels.

Though there is little doubt that the SmartGrid methodology is the future of the power grid, there are significant challenges that remain, but also commercial and sociological as well as scientific and technological. Being outside the scope of this thesis, the commercial and sociological challenges are not discussed herein, though are summarised in [10]. Considering the scientific and technological challenges that are being faced, these range from understanding the interdependency between the digital and the electrical power infrastructures through to the integration and management of large-scale renewable energy sources onto the grid. It is these 'top end' challenges that are being faced that bring us back to the issue of greater flexibility in the power grid. If this is to be achieved, SCC-

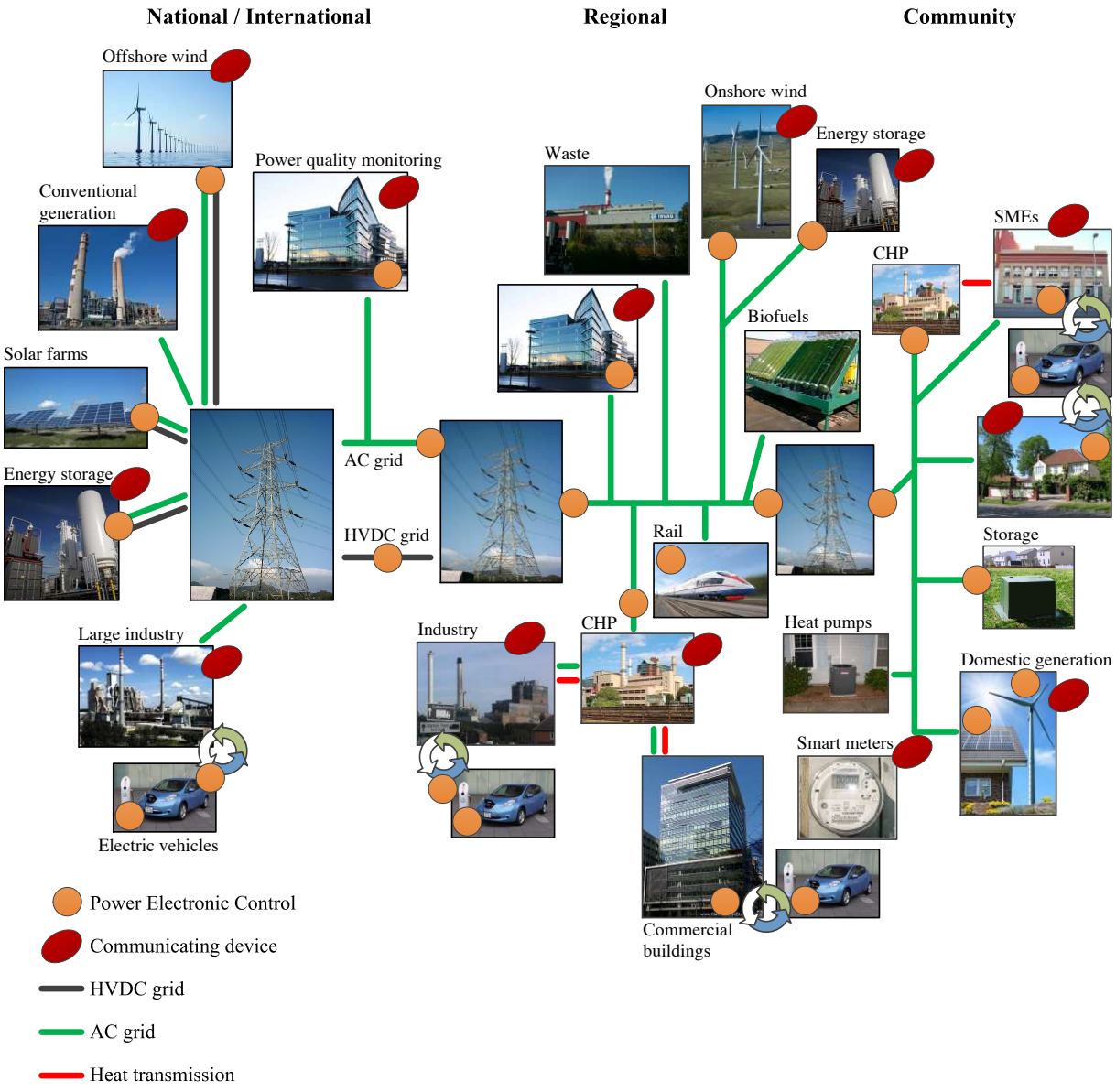


Figure 2.3: The SmartGrid.

type voltage source converter (VSC) circuit topologies, and thus more advanced power electronics, will be required. This is discussed in the next Section.

2.2 Power Electronics for Transmission Systems

Though it was the invention of the high-voltage mercury arc valve (which used mercury vapour in a low pressure chamber to provide current transport and rectifying behaviour) that initially paved the way for the development of HVDC transmission, it was the introduction of solid-state power electronics, initially the thyristor, that really accelerated the development of HVDC technology. It didn't take long for these solid-state devices to displace the use of mercury arc valves in new HVDC schemes across the globe, and, as a result of substantial progress made in the ratings and reliability of thyristor valves in the following years, the competitiveness of HVDC schemes vastly increased. More recently, the introduction of the Insulated Gate Bipolar Transistor (IGBT) has enabled far greater flexibility in power transmission due to its simple turn-off capability. Both of these types of devices, and the power electronics circuits they are used in, are discussed in this Section.

2.2.1 Requirements for Power Electronics Devices

In order for power electronics circuits to perform effectively, the semiconductor devices used within these circuits need to be efficient (typically greater than 95% efficiency), thus exhibiting minimal power losses. Power semiconductor devices are designed to be operated as switches; when 'on', an ideal switch has zero voltage drop across it and will carry any current imposed on it. Conversely, when 'off', the ideal switch will block the flow of current regardless of the voltage across it. In addition, the switching between these

two states should be instantaneous. Put another way, the ideal switch has zero power loss, as the product of current and voltage at any time is zero.

Unfortunately, actual power devices are not capable of this ideal performance, and will always suffer from power losses in both the on and off state as well as during the transition between these two states. In real applications, trade-offs and compromise in performance are necessary; these are dependent on what the particular requirements of the application are. It is to be expected that for power electronics devices used in HVDC systems, the blocking voltages need to be as high as is practically possible, hence a thick, resistive blocking (or drift) region in the device is required. In order to achieve a high blocking voltage whilst at the same time delivering an acceptably low forward resistance, the use of bipolar devices, in which the background resistance of the drift region is reduced by injected carriers (discussed further in Chapter 3), is preferable to unipolar devices, in which the background resistance of the drift region remains the same when in the on-state. However, due to the relatively slow process of electron-hole recombination that takes place in bipolar devices, switching speeds are significantly slower than for unipolar devices. As a result, unipolar devices such as MOSFETs and Schottky barrier diodes (SBDs) find use in low to medium blocking voltage applications, up to around 900 V for commercial Si MOSFETs and around 200 V for Si SBDs. Assuming the use of Si devices, above these voltage levels it becomes necessary to employ bipolar devices such as IGBTs, thyristors and PiN diodes. However, if the use of commercial SiC devices is assumed, the voltage range extends to 1700 V for both MOSFETs and SBDs, with the potential for even greater voltage ratings in the future.

2.2.2 Thyristors and LCC Transmission

The thyristor, first introduced in the mid-1950s and originally known as the silicon controlled rectifier (SCR), is a solid-state device that allows current flow in one direction and blocks in the other, but can also be triggered "on" by an external pulse. The internal structure of the conventional thyristor is shown in Figure 2.4. It can be seen that the thyristor consists of two transistor structures that are connected together, with the collector of a *pnp* transistor forming the base of an *npn* transistor. It is the regenerative action of these two component transistor structures that determines the function of the thyristor. A brief summary of thyristor operation is given herein; a detailed discussion can be found in [11].

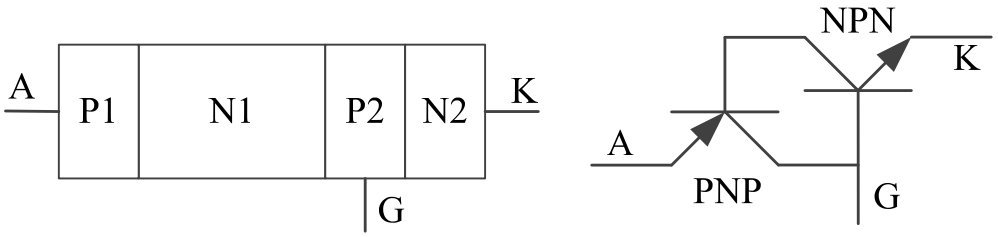


Figure 2.4: Thyristor structure.

With the thyristor forward biased, i.e. the anode (A) is positive with respect to the cathode (K), and with the gate current held to zero, both of the outer p-n junctions are forward biased whilst at the central p-n junction a depletion region builds up, restricting current flow across this junction. This is the forward-blocking, or off-state of the thyristor. In order to turn the device on, a positive current is injected into the gate; this causes the total current flowing out of the cathode to increase. After removal of the gate current, the cathode current must be sufficiently large (greater than the holding current) such that the p- and n-emitters (P1 and N2) inject enough carriers to maintain the device in

conduction.

The regeneration action of the thyristor can be described by considering the two transistors formed by P1-N1-P2 and N1-P2-N2. If the *npn* transistor is turned on by the gate, it supplies current to the *pnp* base, which in turn supplies current to the *npn* base, allowing the gate signal to be removed. At the section of the *pnp* collector and the *npn* collector the anode current can be described as

$$I_A = \alpha pnp I_A + \alpha npn I_K + I_L \tag{2.1}$$

where α represents the transistor current gains, I_K is the cathode current and I_L is the leakage current in the blocking state. Because the cathode current is equal to the sum of the anode and gate currents, the anode current can be redefined as

$$I_A = \frac{\alpha npn I_A + I_L}{1 - \alpha pnp + \alpha npn} \tag{2.2}$$

As such, it can be seen that the thyristor switches to the on-state when the sum of the *pnp* and *npn* transistors is unity. This condition can also be attained without the provision of any gate current, by increasing the applied forward voltage so that carrier multiplication (M>>1) at the N1-P2 junction increases the internal leakage current, which increases the current gains of both transistors. Turn-off of the thyristor requires that, along with zero gate current, the cathode current is reduced to below the holding current level for a certain minimum time; this is achieved by the external current crossing zero (natural commutation) or by forced commutation using additional external components. The current-voltage characteristics of the thyristor are illustrated in Figure 2.5.

Though the conventional SCR-type thyristor is unparalleled with regard to voltage

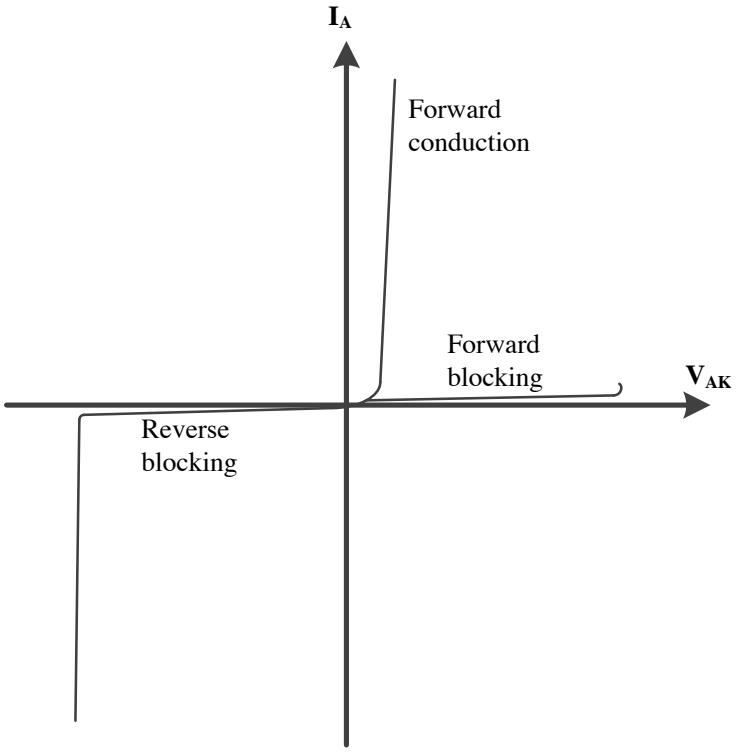


Figure 2.5: Thyristor voltage-current characteristics.

and current ratings of single units, there are several limitations of this device. First, as mentioned previously, is the restriction in turn-off capability of the device. Secondly is a limitation of di/dt, which arises due to the fact that the gate-cathode junction first turns on in the vicinity of the gate contact, taking time for adjacent regions to turn on and thus limiting the safe operating area of the device. If the di/dt is too high, then only part of the thyristor is in conduction, causing excessive heat dissipation in the regions that have turned on and risking device failure. Finally, a third limitation relates to the dv/dt applied to the device, which, if high enough, can create a current which can exceed the holding current of the thyristor and trigger it on. Though the inability to turn-off the thyristor is an inherent feature of the device, design improvements now mean that the

di/dt and dv/dt limitations are less of a constraint; as an example, an 8.5 kV 2180 A Phase Control SCR from Dynex Semiconductor [12] is rated for di/dt of 100 A/μs and dv/dt of 2000 V/μs. However, as outlined in [11], it has been shown that by using excessive gate current under certain operating conditions, it is possible for an inverter SCR to be operated reliably at 10,000-20,000 A/μs.

The lack of turn-off capability of the SCR restricts its practical use to LCC schemes, whereby the source is the AC system voltage. With reference to Figure 2.6, LCC is reliant on the natural current zeroes that are created by the external circuit in order to transfer current from switch to switch. This operation is explained with the aid of Figure 2.7. Here, an approximated DC voltage is obtained from the three-phase AC voltage as the SCRs are cycled on in pairs, as described at the top of the Figure. The firing delay angle of the SCRs is denoted here by α; it is noted that $\alpha = 0$ gives identical operation to a three-phase diode rectifier. This converter acts as a rectifier for firing delay angles from 0 to $\pi/2$, giving a positive output, whilst for firing delay angles from $\pi/2$ to π the converter acts as an inverter, giving a negative output.

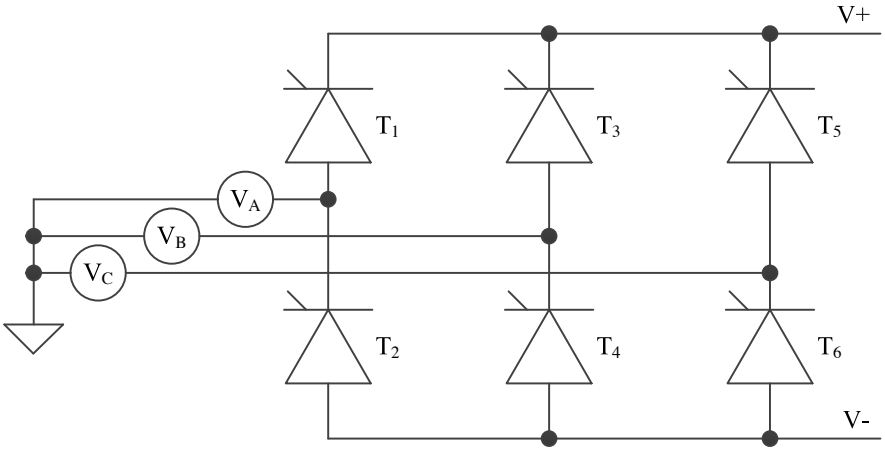


Figure 2.6: Schematic of an SCR-based three-phase converter.

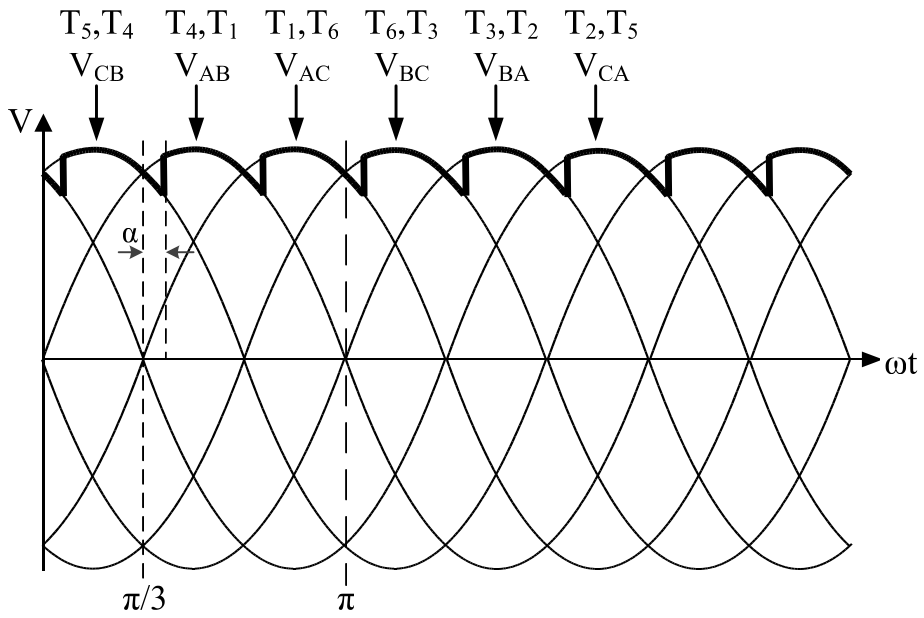


Figure 2.7: Operation of a SCR-based three-phase converter.

Although this is the least flexible solution for DC transmission, it was, until very recently, still the most common solution due to its relative maturity when compared to SCC schemes. Unfortunately, though the LCC configuration is simple, it has significant shortcomings in the form of large reactive power requirements, injection of low-order harmonic currents, risk of inverter commutation failures and the dependence on strong AC systems for the provision of commutation voltages. As mentioned previously, the use of SCC schemes which utilise more advanced power electronics devices can eliminate these problems. This has meant that, nowadays, LCC schemes are typically only employed for very long distance point-to-point bulk power transmission at voltages in excess of 320 kV, where the advantages of SCC transmission are not required. At the current time, IGBT-based VSC is the favoured SCC technique for HVDC technology; as such, this is discussed in the next Section.

2.2.3 IGBTs and SCC Transmission

The IGBT, first experimentally demonstrated in 1979 [13], combines the voltage-driven high-impedance and low-power gate of MOSFET technology with the power handling capability of bipolar junction transistors (BJTs) and thyristors. However, it wasn't until the 1990s that its feasibility for high voltage applications was realised. The internal structure of the IGBT, and its equivalent circuit, is illustrated in Figure 2.8. The structure is identical to that of a MOSFET, except for the highly doped p-type layer located at the collector of the device, which acts as a p-type emitter of a *pnp* BJT to the drain of the MOSFET. The BJT is driven by electrons from the MOS channel which provide the base current, and holes are injected from the p-type emitter. Like with a MOSFET, a voltage bias on the gate results in the inversion of the p-type region directly underneath the gate oxide layer; this results in the formation of a shallow channel region which allows current flow from the collector to the emitter.

With reference to the equivalent IGBT circuit shown in Figure 2.8, the most significant breakthrough in the development of IGBT technology was obtaining a low shorting resistance (R_S) between the emitter and base of the *npn* transistor (in the p-type regions underneath the emitters) to minimise the risk of the parasitic *pnpn* thyristor (formed by the $P+/N-/P-/N+$ junctions from the collector to the emitters) latching up. This latch up condition could occur at high voltages, when the level of electrons injected from the n-type emitters can turn on the parasitic thyristor. The latching up of an IGBT is an undesirable condition, as the collector current is no longer controlled by the gate, and the device can only be turned off in the same manner as the conventional thyristor. However, unlike with the thyristor, this turn-off has to be done quickly in order to prevent excessive power dissipation permanently destroying the IGBT. The required low shorting resistance

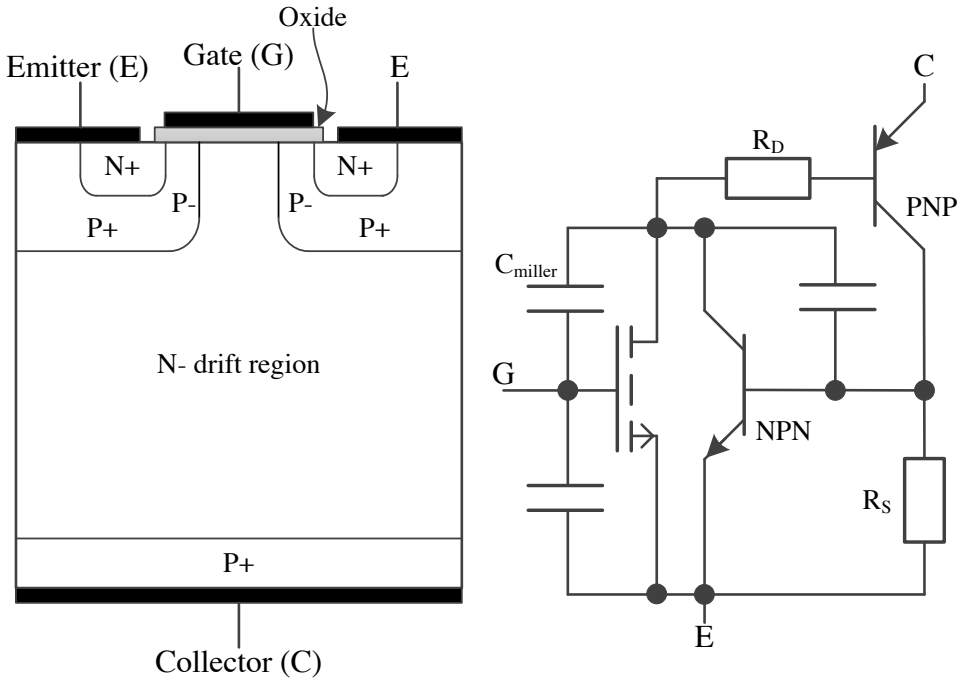


Figure 2.8: IGBT structure and equivalent circuit.

for minimising the risk of latch up is achieved by controlling the doping profiles within the device to ensure that the *npn* section of the parasitic thyristor cannot turn on.

As with MOSFET devices, IGBTs are fabricated in a cellular topology, meaning that when the device is turned on, the problem of slow current spreading that is observed in the conventional thyristor is avoided. Furthermore, when the gate voltage is removed to turn the device off, the base drive current is cut off, allowing a depletion region to quickly form at the emitter *pn* junction; as such, the turn-off delay of the IGBT is much less than than the storage time in BJT devices. Another advantage of the IGBT is that it is possible to exercise linear control through the gate, meaning that di/dt and dv/dt can be controlled during the commutations. This in turn means that there is no need for a di/dt limiting reactor in the circuit, unlike for the gate turn-off (GTO) variant of the thyristor.

With the use of IGBTs, the flexibility of HVDC transmission systems can be greatly enhanced by using SCC VSC-based power conversion, and the problems associated with CSC-LCC transmission, outlined in Section 2.2.2, are eliminated. VSC-based transmission allows the flow of active power and the provision of reactive power in both directions at each end of the HVDC link, which is particularly advantageous for cable transmission, as the absence of polarity reversal means that the cable design is greatly simplified [14]. SCC-VSC also has the benefit of not requiring an AC system voltage source for the commutations, and can be controlled to generate or absorb reactive power independently from the active power flow. Furthermore, the generation of harmonics is greatly reduced in VSC-based systems, due to the relatively poor quality of LCC waveforms, meaning that the requirement for filters is either eliminated or their size allowed to be reduced to absorb only the higher harmonics. Finally, because the direction of current flow can be changed, fast power reversal at each terminal of a HVDC scheme is achievable without the need for switching operations.

Though VSC-based systems have clear benefits in terms of the flexibility of power transmission when compared to conventional thyristor-based LCC systems, they are not without their disadvantages. In the LCC system, due to the combination of peak current-limiting smoothing reactors and fast converter control, which quickly reduces the DC current to zero, the response to DC system faults is rapid, and a restart is possible in less than 300 ms. However, in a VSC system, the presence of the free-wheeling diodes means that the fault current is allowed to continue indefinitely even when the IGBTs are turned off. As such, the fault can only be cleared by the use of circuit breakers, thus meaning that large delays in restoring normal system operation will be realised. Another disadvantage of VSC when compared to LCC is that, due to the high frequency pulse width modulation (PWM) switching of the IGBTs, the power losses in VSC systems are substantially higher

than in LCC systems. However, by using multi-level conversion techniques [15] instead of PWM-based VSC, these power losses can be greatly reduced, as the main IGBTs within the multi-level converter (MLC) are switched at the fundamental frequency, meaning the higher frequency components typical of PWM are eliminated. In [16], where a MLC based on SiC junction field-effect transistors (JFETs) has been investigated, efficiencies of 99.8% have been reported.

2.2.4 The Role of the PiN Diode

In addition to the IGBT switching devices, junction rectifiers, or diodes, are are also required in a SCC circuit, connected in anti-parallel to the IGBTs to ensure that the bridge voltage has a single polarity whilst allowing the current to flow in both directions. The diode can be considering as the fundamental building block of semiconductor devices, consisting of a *pn* junction to allow current to flow in one direction whilst blocking it in the opposite direction. However, for the high voltage applications that are relevant to this work, the *pn* junction diode is extended to include a low-doped 'intrinsic' ('*i*') region sandwiched between the p- and n-type regions, providing the required blocking voltage capability. This *p*-*i*-*n* structure gives rise to the term PiN diode, which is used from hereon in this thesis. Being the subject of this thesis, a comprehensive discussion of the high voltage PiN diode is given in Chapter 3.

2.3 Silicon Carbide for Power Electronics

At the present time, the majority of power semiconductor devices are fabricated using silicon (Si) as the base material. High-quality monocrystalline Si is widely available at low cost, and its physical properties and manufacturability have allowed the successful

development of both unipolar and bipolar devices. However, though its physical properties allow it to perform well at modest temperatures (typically less than 125°C), it is unsuitable for modern applications which demand increasingly higher power density and temperature operation. For such applications, the use of wide band gap semiconductor materials is attractive. As well as SiC, other wide band gap materials, such as gallium nitride (GaN) and diamond (C), have been the subject of considerable global research in recent years. However, as a result of its relative maturity compared to GaN and C, in addition to it having a native oxide (SiO_2) and acceptable mobilities in both n- and p-doped material, SiC appears to be the most likely successor to Si for high voltage power electronics applications.

2.3.1 History of Silicon Carbide

The scientific history of SiC begins in 1824, when the Swedish chemist Jöns Jacob Berzelius suggested that a Si-C chemical bond might exist. However, it wasn't until several decades later, in 1891, that Eugene G. Acheson established a process for making commercial quantities of SiC (then termed "carborundum") whilst attempting to synthesise diamond. Acheson subsequently patented this method for making powdered SiC, as well as developing the electric batch furnace by which bulk SiC has been manufactured ever since. Due to the inherent hardness of the material, early applications of SiC were as an abrasive; the use of SiC for this type of application is still widely prevalent today.

Electronic applications of SiC soon followed the aforementioned mechanical abrasion applications. In 1907, Henry J. Round produced the first light emitting diode (LED) by applying a voltage to a SiC crystal and observing yellow, green and orange luminescence at the cathode. Around this time, SiC crystals also found use as detectors in early radio

receivers, as outlined in the USA patent by Henry H. C. Dunwoody [17]. In the years soon after this, it was suggested by Baumhauer [18, 19] that SiC could crystallise in a range of different forms, varying only in the stacking order in a single direction, a phenomenon he termed "polytypism" (discussed further in Section 2.3.2).

It was a little over forty years later, in 1955, when Jan Antony Lely at Philips (Eindhoven, Netherlands) developed a method for producing high quality SiC crystals that had potential for the semiconductor industry [20]. This breakthrough in crystal growth spurned a growth in interest in using SiC as an electronic material, and, soon after, the first SiC conference was held in Boston, USA, in 1958. The next major breakthrough in SiC research didn't come until 1978, when the use of a seeded sublimation growth technique (also known as the modified Lely technique) was demonstrated by Tairov and Tsvetkov [21]. It was this breakthrough that led to the possibility of realising bulk SiC crystals.

Soon after this, Matsunami et al. [22] demonstrated the growth of cubic SiC on Si substrates, triggering a wealth of research in this area in the following years. In 1987, Cree, Inc. [23], the first commercial supplier of SiC substrates, was founded. Five years after this, in 1992, Bhatnagar et al. [24] reported the first high-voltage (400 V) SiC Schottky barrier diodes, this work demonstrating the superior electrical performance offered by these devices when compared to high-speed Si rectifiers with similar voltage ratings. The first multi-kV $p^{+}n$ junction SiC device soon followed in 1994 [25], successfully blocking 2 kV. This was surpassed by Kordina et al. [26] in 1995, who reported a SiC rectifier capable of blocking 4.5 kV.

In 1996, the voltage blocking capability of SiC Schottky rectifiers was extended to 1750 V by Itoh et al. [27]; five years after this, in 2001, commercialisation of SiC Schottky diodes was announced by Cree, Inc [23], Infineon Technologies [28], Microsemi Co. [29],

and IXYS Co. [30]. The following year saw Cree, Inc. introduce their 600 V, 20 A "Zero Recovery" SiC Schottky rectifier, and 2003 saw the release of their first commercial 1200 V SiC Schottky rectifier. This year also saw Cree, Inc. demonstrate 100 mm semi-insulating SiC substrates, enabling greater yields, and hence reduced costs, for MESFET devices fabricated on such substrates.

In 2004, researchers at Toyota Central R&D Laboratories, Inc. and DENSO Co. reported a novel 'repeated *a*-face' (RAF) growth process for realising SiC substrates with massively reduced dislocation densities compared to previous conventional substrates [31], enabling large size substrates; this in turn enabling feasible commercial applications. This breakthrough was soon followed by the commercial introduction of 100 mm SiC substrates and epitaxy material from Cree, Inc., in 2005. Developments in substrate processing techniques culminated in the commercial release of 100 mm, Zero Micropipe SiC substrates from Cree, Inc. in October 2007, enabling greater device yield from this premium-grade material.

Recent years have seen several other SiC substrate manufacturers, such as Norstel [32], II-VI [33], Dow Corning [34] and TanKeBlue [35] enter the marketplace with their own substrates and epitaxy services. Given the relatively high cost of SiC substrates compared to their Si counterparts, this increased competition, along with increasing demand and substrate size, can only have a positive effect in reducing the cost of SiC material and devices. Increasing demand has been observed, predominantly due to the success of the SiC SBD. That said, due to the predominantly power application-specific nature of SiC devices, it is unlikely that demand will ever reach that of Si devices, thus it is expected that there will always be some difference in cost maintained. As such, it will be crucial for SiC to justify this cost difference, by proving the efficiency savings in the end-product (such as an inverter), for example. On the subject of substrate size, Cree, Inc. announced

a 150 mm SiC wafer in August 2012; for comparison, the Si industry uses 300 mm wafers as the current standard, with research underway into developing a 450 mm technology [36].

2011 saw what was perhaps one of the most important milestones for SiC technology in recent years, with Cree, Inc. introducing the industry's first fully qualified commercial SiC power MOSFET, rated for 1.2 kV operation [37]. Since the release of their first commercial SiC MOSFET, Cree have extended their range of available devices to include a 2nd generation 1.2 kV MOSFET, as well as 1.2 kV SiC power modules. In addition to Cree, other device manufacturers that have recently entered the SiC power device market include Fairchild Semiconductor [38], who, by taking over TranSiC in 2011, have acquired their SiC bipolar junction transistor (BJT) expertise and are expected to release a 1.2 kV power BJT device in the near future. As of 2013, Rohm Semiconductor [39] have also released a range of SiC MOSFETs and power modules, again targeting the 1.2 kV application range. A more detailed discussion of the current status of SiC power devices is given in Section 2.3.5.

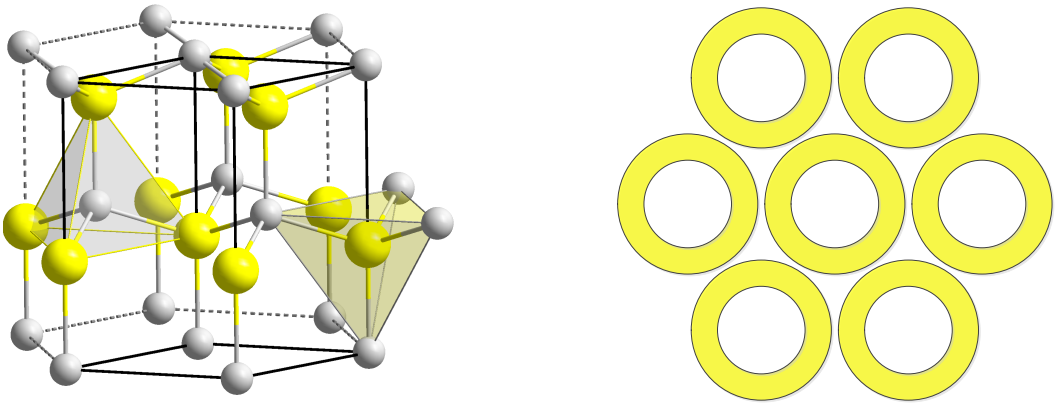
2.3.2 Polytypes of Silicon Carbide

As mentioned previously, SiC occurs in many different crystal structures, known as polytypes. Though each of these polytypes consist of an equal number of covalently-bonded Si and C atoms, each polytype has distinct electrical properties. A comprehensive introduction to SiC polytypes is given by Bechstedt et al. [40]. As of 2006, over 250 different polytypes of SiC had been identified [41], though only a handful of these are commonly grown in a reproducible form suitable for use as an electronic-grade semiconductor. The cubic polytype 3C-SiC and the hexagonal polytype 4H-SiC are the most common SiC polytypes presently being developed for semiconductor devices, due to their superior

electrical properties (discussed in Section 2.3.3). Other polytypes that have also been investigated for their electrical properties include hexagonal polytypes 2H- and 6H-SiC, and the rhombohedral polytype 15R-SiC.

It is found that SiC crystallises in the wurtzite lattice form, the structure of which is illustrated in Figure 2.9(a). This crystal structure consists of interpenetrating hexagonal close-packed lattices in which Si and C atomic layers alternate, meaning that every Si atom has four neighbouring C atoms, and vice versa. The hexagonal layers of Si atoms with C atoms located directly above are illustrated in Figure 2.9(b), for a single Si-C layer of atoms. This is expanded in Figure 2.10 to show two Si-C atomic layers, and illustrates the polymorphism of SiC. It can be seen that there are two possible locations for the second layer of Si-C atoms, labelled B and C, which are 60° apart relative to the position of Si-C layer A. The position of the second, and then subsequent Si-C layers is what defines the polytype of SiC, thus each polytype is identified by a unique stacking sequence. The stacking sequences of the common SiC polytypes are illustrated in Figure 2.11.

Of particular interest to this work, the polytype 4H-SiC is found to have the four layer repeating stacking sequence ABCB, and its crystal structure consists of 1/2 hexagonal and 1/2 cubic sites. This is in contrast to the 6H-SiC polytype (the only other polytype with substrates commercially available), which, with a stacking sequence of ABCACB, and 1/3 hexagonal to 2/3 cubic sites, exhibits more anisotropy in its material characteristics. It is this anisotropy in material characteristics, particularly the carrier mobility, that have led to 4H-SiC being preferred over 6H-SiC for power semiconductor devices in recent years. Another polytype that has gained great interest in recent years is the cubic polytype 3C-SiC. It is the cubic nature of 3C-SiC that is attractive, as it can be grown on a substrate such as Si, and thus potentially offers a low cost alternative to 4H-SiC, albeit with a lower



(a) (b)

Figure 2.9: Crystalline structure and hexagonal packing system of SiC; yellow atoms are Si, white atoms are C. (a) shows the wurtzite formation of crystalline SiC and (b) illustrates the hexagonal packing of a single Si-C layer.

energy band gap and hence lower maximum operating temperature and voltage.

2.3.3 Thermal and Electrical Properties of Silicon Carbide

It is the superior thermal and electrical properties of SiC that have made it attractive for use a semiconductor device material, in particular for power electronics applications. A comparison of the key electrical properties of the 3C- and 4H-SiC polytypes against other wide band gap semiconductor materials as well as Si is given in Table 2.1. One notable difference in the characteristics of Si when compared against the wide band gap semiconductors is the significantly larger intrinsic carrier concentration. It is this property that limits Si device operating temperature to around 150°C [42]. At this temperature, Si has acquired sufficient energy for the number of thermally generated electron-hole pairs to exceed the number of free carriers which are present due to the intentional doping of the material. At this point, the material becomes intrinsic and the device fails. In contrast, the wide band gap of 4H-SiC allows it to reach temperatures of around 700°C

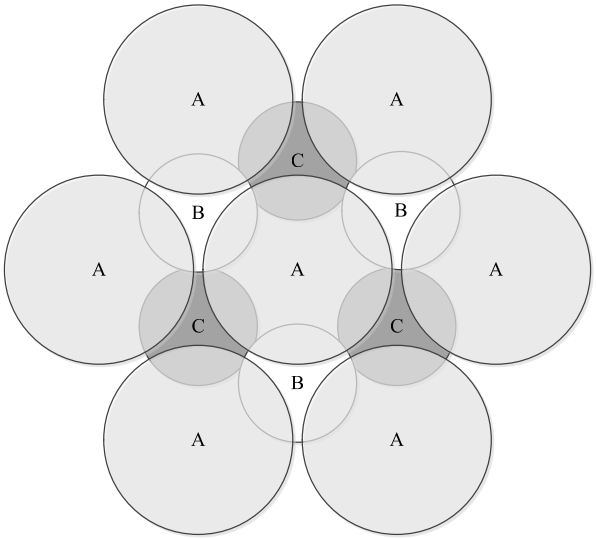


Figure 2.10: The hexagonal packing system in SiC; Si-C layer 1 atoms are identified as A and the subsequent Si-C layer is either in position B or C.

before operating in the intrinsic region. Based on current technology, this temperature far surpasses the capability of any semiconductor device packaging, and is similar to or higher than the melting point of conventional metals used for wire bonding, such as aluminium, gold and copper. For now at least, the limitation for high temperature SiC remains due to these packaging technology constraints.

Table 2.1: The material properties of Si, C, 4H-SiC, 3C-SiC and GaN at 300 K [43]. The mobility values shown for 4H-SiC and GaN are those along the a-axis.

Property	Units	**Si**	**C**	**4H-SiC**	**3C-SiC**	**GaN**
Bandgap Energy, E_G	eV	1.12	5.5	3.26	2.2	3.39
Critical Field, $\mathscr{E}_C$	MV/cm	0.3	10	3-4	2-3	5
Int. Carrier Conc., n_i	cm^{-3}	$\approx 10^{10}$	$\approx 10^{-27}$	$\approx 10^{-8}$	$\approx 10^{1}$	$\approx 10^{-10}$
Dielectric Constant, ε_r		11.8	5.5	9.7	9.6	9.9
Thermal Conductivity, λ	W/cm-K	1.5	20	4.5	4.5	1.3
Elec. Sat. Velocity υ_{sat}	10^7cm/s	1.0	2.7	2	2	2.5
Electron Mobility, μ_n	cm^2/V-s	1350	1900	720	900	1000
Hole Mobility, μ_p	cm^2/V-s	450	1200	120	320	350

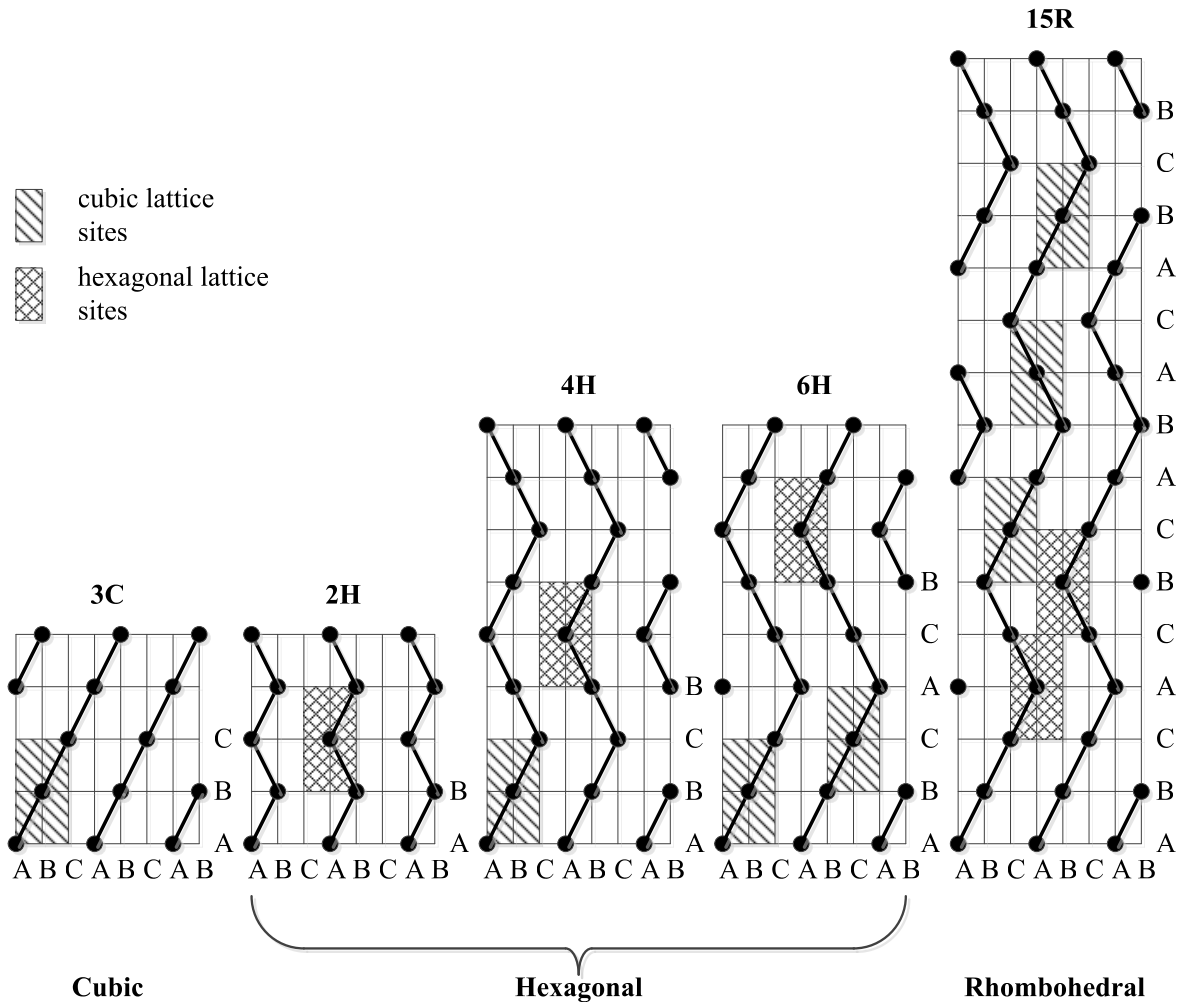


Figure 2.11: Polytypes of SiC.

Another key observation from the above comparison is the high critical electric field for 4H-SiC, which is approximately ten times greater than that for Si. The value of critical electric field for a semiconductor material is proportional to the band gap energy; a wider band gap means that a higher energy is required to break a chemical bond, thus allowing larger electric fields to be applied before avalanche multiplication of ionised carriers ensues. The greater critical electric field strength of 4H-SiC compared to Si means that for the same device width, 4H-SiC can withstand around ten times the voltage before the electric field strength reaches a level sufficient to accelerate carriers and cause impact ionisation in the semiconductor (this is discussed in more detail in Chapter 3). This means that, with respect to a Si device, a much thinner, more highly doped 4H-SiC 'drift' region can be used without compromising blocking voltage capability. This is illustrated in Figure 2.12, which shows the theoretical unipolar limit of specific on-resistance against breakdown voltage for a given drift region design. It can be seen from this Figure that 4H-SiC devices offer specific on-resistances of the order of 350 times lower than their Si counterparts. Furthermore, the fact that 4H-SiC devices can be fabricated with thinner drift regions means they can be operated at higher frequencies, as well as enabling lower switching losses, due to the lower carrier lifetime of 4H-SiC (discussed further in Chapter 3). Low switching losses are also aided by the superior electron saturation velocity of 4H-SiC, which is approximately an order of magnitude higher than that for Si.

It is evident from Figure 2.12 that the Si 'super-junction' (SJ) theoretical limit surpasses that of the Si unipolar limit. This would correspondingly apply to any semiconductor material; as such, it is worthwhile to discuss the operating principles that make this possible. The SJ device structure is identical to that of a standard MOSFET, with the exception of alternating p- and n-type columns in the drift region (as opposed to a single p- or n-type region). This charge-coupled structure means that when a positive

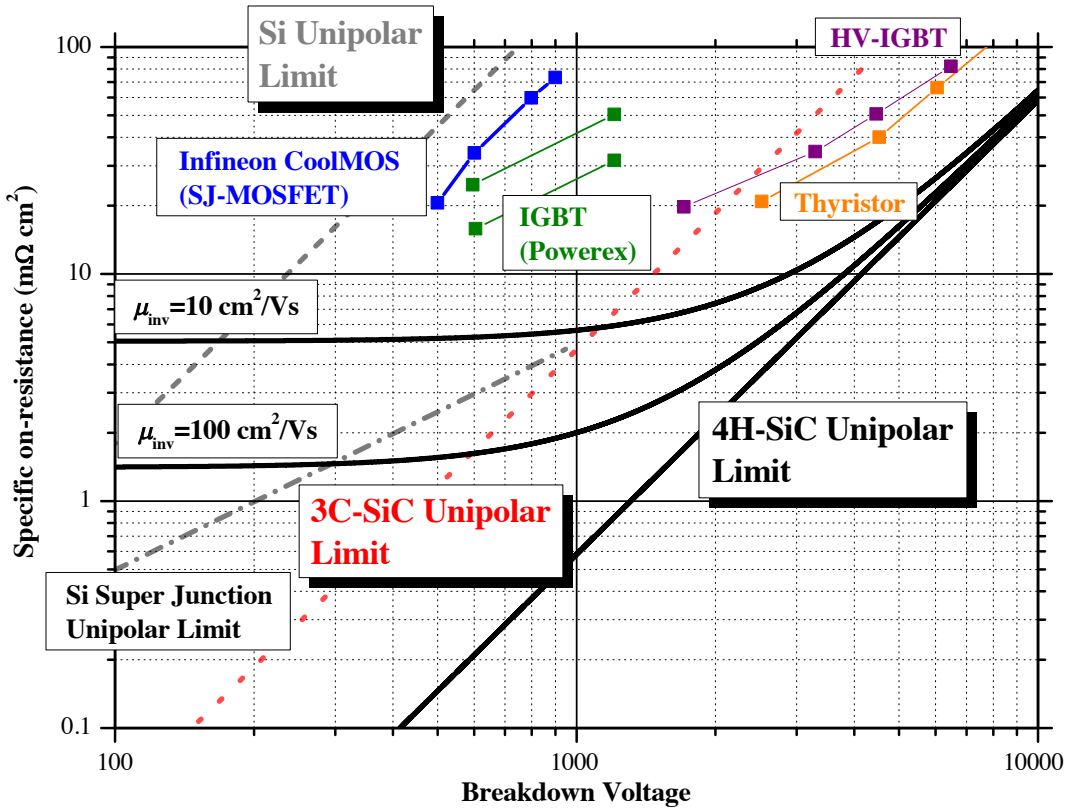


Figure 2.12: Theoretical unipolar limits of Si, 3C-SiC and 4H-SiC. Also shown are the calculated limits for MOS inversion channel mobilities of 10 cm^2/V-s and 100 cm^2/V-s, as well as the measured specific on-resistance of a range of Si devices.

bias is applied to the MOSFET drain with zero gate bias, vertical junctions are formed between the p- and n-type columns of the drift region, Simultaneously, horizontal junctions are formed between the p-type drift region and the n-type buffer layer as well as between the gate electrode on the upper surface of the n-type drift region. This results in depletion regions being formed across the vertical junction as well as the horizontal MOS interface, creating a two-dimensional charge-coupling phenomenon. This two-dimensional depletion region alters the electric field distribution in the vertical direction from the triangular shape observed in conventional parallel-plane junctions to a rectangular shape.

As such, the SJ device can achieve a higher blocking voltage for a given drift region thickness. Moreover, the doping concentration in the n-type drift region can be made higher than that predicted by the one-dimensional theory, meaning that a reduction in specific on-resistance can be achieved. However, it is crucial that a precise charge concentration is achieved for the p- and n-type drift region in order for the SJ device to achieve a high breakdown voltage [44].

The high thermal conductivity of 4H-SiC, which is approximately three times higher than that for Si and similar to that of copper, is another important advantage for power electronics applications, as it means that 4H-SiC devices can be operated at higher power densities, and will dissipate heat much more readily, thus reducing the requirement for large, bulky heat sinks and cooling apparatus. Furthermore, the long-term reliability of the device is also benefitted by this, as it is possible to operate the device at a constant maximum output power. Lastly, as mentioned above, the very low intrinsic carrier concentration of 4H-SiC also benefits high temperature operation of power devices.

One disadvantage of 4H-SiC when compared to Si that is evident from Table 2.1 is the lower carrier mobility (both electrons and holes) in the material. A lower mobility corresponds to higher on-resistance, and thus increased on-state losses. However, as mentioned previously, the on-state resistance in a 4H-SiC unipolar device is aided by the fact that a thinner, more highly doped drift region can be employed, thus mitigating this disadvantage. It is important to note here that the values for mobility outlined in Table 2.1 are for the bulk material; unfortunately, due to the poor quality 4H-SiC/SiO_2 interface, the surface mobility in 4H-SiC is significantly lower than in the bulk of the material [45]. This has significant implications in particular for MOS devices, as the low surface mobility leads to a high channel resistance, and hence high on-state losses.

2.3.4 Bulk Material Challenges

Due to the extremely high pressures and temperatures that would be required to grow single crystal SiC using conventional crystal pulling techniques as used in the Si semiconductor industry, calculated to be above 10^5 atm and 3200°C for pressure and temperature respectively [46], such techniques are rendered impractical for commercial production of single crystal SiC. As such, several other approaches have been investigated, in order to enable commercial production of large diameter semiconductor-grade SiC. The most popular approach is that developed by Lely [20] and subsequently extended by Tairov and Tsvetkov [21], and is generically referred to as the Physical Vapour Transport, or PVT, process. Another important SiC growth technique is High Temperature Chemical Vapour deposition (HTCVD) [47], which allows SiC boules to be grown with very low impurity levels, at growth rates comparable to the PVT process (up to 1 mm/hour).

Though significant progress has been made in reducing the defect densities of SiC substrates over the past two decades, this is still perhaps the most critical challenge faced by SiC wafer technology, and is continuing to hinder the development of large area high current and high voltage devices. Types of defects in nominally <0001> grown SiC include:

1. Polytype instabilities.
2. Open-core dislocations (micropipes).
3. Low-angle grain boundaries.
4. Conventional dislocations.
5. Point defects (discussed in Chapter 3).

Addressing each of these types of defect in turn, the polytype instability defect will first be discussed. As outlined in Section 2.3.2, the difference between SiC polytypes is the

stacking sequence of the Si-C bi-layers in the <0001> direction. As such, if the polytype is to remain the same throughout the entire crystal, the stacking sequence must remain involatile. However, due to the low stacking fault energy of 4H-SiC, it is difficult to suppress parasitic polytype formation and thus to grow a single polytype crystal [48]. Furthermore, the presence of other types of defects also adds to the problem, as not only can polytype inclusions lead to the formation of other defects, but these defects can also result in polytype disturbances [49]. In order to prevent this polytype inclusion, themal conditions and growth pressures need to be precisely controlled, and attention has to be paid to the design of the growth cell and mounting of the seed crystal [50].

Until fairly recently, the micropipe defect was the scourge of SiC substrates, gaining a fearsome reputation as a 'killer defect' due to its ability to prevent a SiC device from blocking a reverse voltage, thus potentially rendering it useless. Illustrated in Figure 2.13, a micropipe is the hollow core of a large screw dislocation, which penetrates the entire crystal along the growth direction (parallel to the c-axis) and is replicated to the epitaxial layer(s) of the device. As such, the epitaxy quality is heavily dependent on the quality of the initial substrate. However, as discussed in Section 2.3.1, improvements in the sublimation growth method for bulk SiC [51] resulted in the micropipe density in 4H-SiC substrates having decreased dramatically, leading to the availability of micropipe-free substrates.

When large diameter SiC crystals are grown under non-optimised process conditions, the formation of low-angle grain boundaries (LAGBs) can occur. These LAGBs are defined as the boundaries between misaligned regions of the SiC material, and generally consist of threading edge and screw dislocations, the implications of which are discussed below. Furthermore, LAGBs can act as stress concentrators which can result in wafer cracking at defect locations during the epitaxial growth process. Fortunately, the density

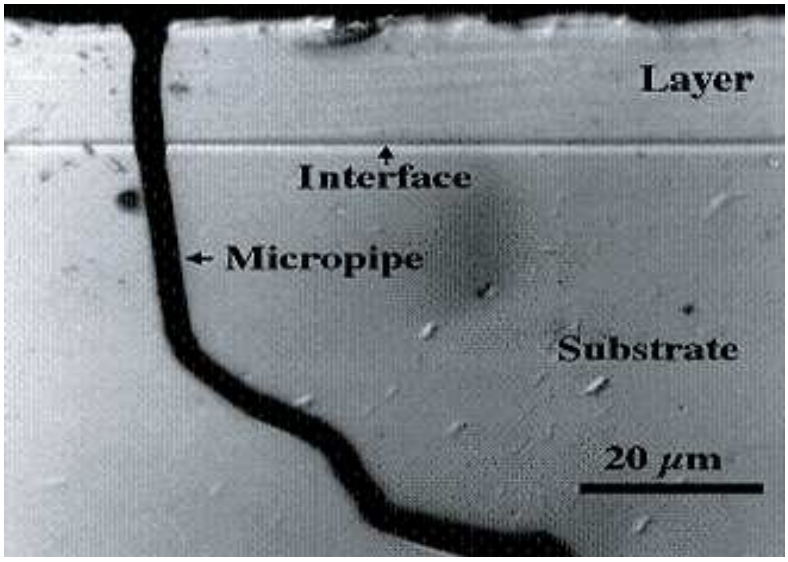


Figure 2.13: Cross sectional view of a micropipe emanating from the substrate and propagating into the epitaxial layer.

of LAGBs in commercial SiC material has been drastically reduced in recent years [46].

Next to be discussed is the conventional dislocation defect. However, this term encompasses several types of defect, including the previously discussed micropipe, threading screw dislocations (TSDs), threading edge dislocations (TEDs) and basal plane dislocations (BPDs) [46]. These dislocations are illustrated schematically in Figure 2.14. As discussed in [52], the density of TSDs in good quality epitaxial films is of the order $\sim 10^3$ cm^{-2}, thus posing a problem for SiC power devices, as they have been found to result in increased reverse leakage currents and lower reverse breakdown voltages in 4H-SiC devices [53]. Furthermore, as illustrated in Figure 2.14, it is possible for TSDs to spawn other defects, such as the carrot defect.

Similar to the TSD, the TED is a defect that can also propagate into epilayers, and are typically found in 4H-SiC substrates at a density of the order $\sim 10^4$ cm^{-2} [46]. As outlined by Maximenko et al. [52], the effect of TEDs on device performance is unclear, though

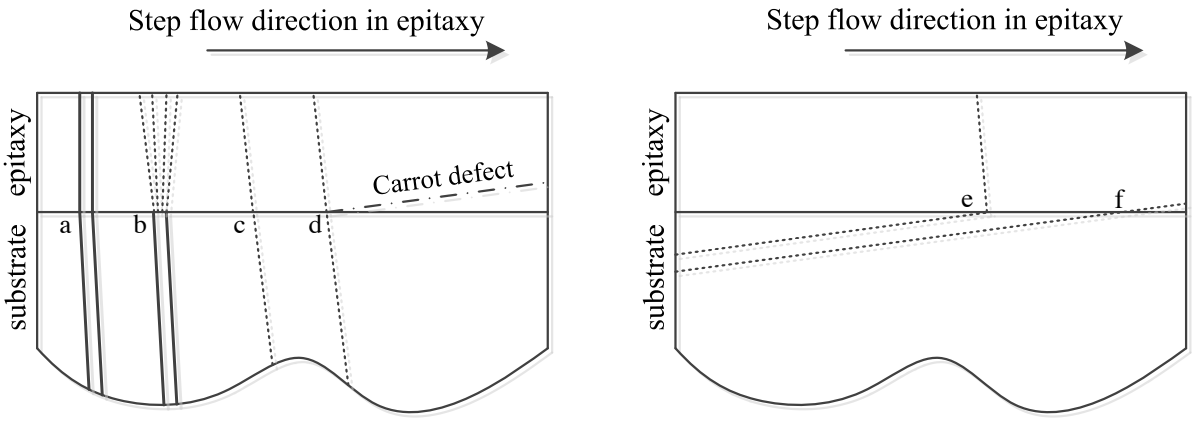


Figure 2.14: Propagation of substrate defects into epitaxial layer a) micropipe, b) micropipe to multiple closed core TSDs, c) TSD, d) TSD to carrot defect and TSD, e) BPD to TED, f) BPD.

available experimental data has proved that TEDs (as well as TSDs) serve as efficient recombination sites, thus degrading the carrier transport properties of the material.

The remaining dislocation-type defect to discuss here, and one that has particular relevance for bipolar 4H-SiC devices, is the BPD. In order to take advantage of step-flow growth, SiC epitaxial layers are typically grown on substrates that are cut off-axis by 4-8°, meaning that the basal plane of the crystal is tilted with respect to the surface of the wafer. As such, as illustrated in Figure 2.14(f), BPDs can propagate from the substrate into the epitaxial layer. As observed in the work by Stahlbush et al. [54], propagation of stacking faults caused by BPDs can compromise the reliability of 4H-SiC devices. This stacking fault propagation is caused by the energy released by the action of electron-hole recombination in the conductivity-modulated region of 4H-SiC bipolar devices, and, as the propagation of these faults increases during forward bias, the level of conductivity modulation decreases, thus resulting in a forward voltage drift of the device. Though this is a serious problem for bipolar devices, it is found that most BPDs that are present in

the 4H-SiC substrate are converted to more benign TEDs during epitaxial growth [55]. Furthermore, as of September 2012, Cree, Inc announced the commercial introduction of 100 mm 4H-SiC epitaxial wafers with a total BPD density of < 1 cm^{-2} [56], enabling bipolar 4H-SiC devices to have improved stability over time.

2.3.5 Current Status of Silicon Carbide Power Devices

At the current time, the only types of SiC devices that are commercially available are MOSFETs and Schottky diodes, with maximum voltage ratings of 1200 V and 1700 V respectively. Only two manufacturers, namely Cree, Inc. and Rohm Semiconductor have SiC MOSFETs in the market; these two manufacturers also have Schottky diodes available, along with Infineon Technologies. Looking first at the status of the commercially available MOSFET devices, it is evident that the electrical performance of the devices from Cree, Inc. and Rohm Semiconductor are almost identical; notably they both quote a specific on-resistance ($R_{DS(on)}$) value of 80 mΩ. However, the devices available from Rohm Semiconductor allow a maximum operating temperature of +150°C; this compares to a value of +135°C specified by Cree, Inc.

As has been outlined in Section 2.3.3, the on-resistance of SiC MOSFETs is predominantly governed by the high channel resistance, which arises due to the low channel mobility which results from the presence of an oxycarbide region at the SiC/SiO_2 interface, resulting in very high near interface trap densities (D_{it}) [57]. Technological developments in the field of interface passivation, specifically the application of nitric oxide (NO) post-oxidation annealing, have allowed the commercialisation of SiC MOSFET devices by providing an acceptable channel mobility of around 35 cm^2/V·s. However, this is still only around 4% of the mobility in the semiconductor bulk. More recently, Sharma et al. [58]

have presented a phosphorous (P) passivation technique which provides a channel mobility of around 70 $cm^2/V{\cdot}s$, as well as improved threshold voltage stability when compared to previous methods utilising phosphorous passivation.

To date, no bipolar SiC semiconductor devices have been commercially released as yet, though, as mentioned in Section 2.3.1, Fairchild Semiconductor look set to release a 1.2 kV BJT in the near future. For BJTs to be viable alternatives to MOS-based devices such as MOSFETs and IGBTs, their current gain needs to be sufficiently high across the operating temperature range so that the current for the base drive circuit is minimised. The highest values of current gain achieved in 4H-SiC BJT techology have been reported by Miyake et al. [59], who, by using optimised device geometry, optimised surface passivation and continuous epitaxial growth, achieved current gains of 257 and 335 on (0001) and (000-1) orientated 4H-SiC material, respectively. However, the BJT devices fabricated in this work did not include any edge termination, and were thus not capable of blocking a significant voltage. More recently, the same research group have reported 4H-SiC BJTs with a rated blocking voltage of 20 kV [60]. This is the highest value of blocking voltage reported for a 4H-SiC power switching device ever reported, and demonstrates the effectiveness of the edge termination technique that has been developed by this research group.

Before 4H-SiC BJTs can enter the commercial market, it is crucial that their stability over time is proven. Researchers at GeneSiC Semiconductor [61], who are developing 4H-SiC BJTs with 1.2 kV to 10 kV ratings, have recently published a study of the long-term operating stability of their devices [62]. The devices that were studied in this work were 1.2 kV/5 A-rated BJTs, with an active area of 2.95 mm^2, under long-term avalanche mode, DC, and pulsed current operation at temperatures ranging between 25°C and 125°C. It was found that, although the current gain was stable over time at 25°C during DC tests,

at increased operating temperatures degradation of the current gain of the BJTs was observed, with the gain dropping to around 75% of the initial pre-test value after 5.8 hours at 125°C. However, it was also found that after around 25 hours of DC testing the current gain value approached a steady-state value, suggesting that the gain could be stabilised after a device burn-in process. Furthermore, it was found that the current gain of degraded devices could be recovered after a thermal anneal at 240°C, suggesting that the device performance could be recovered *in situ* by operating them in pulsed mode at temperatures greater than 200°C.

GeneSiC Semiconductor are also heavily involved in the development of 4H-SiC thyristors, targeting 6.5 kV to 13 kV applications, as well as Cree, Inc. and United Silicon Carbide, Inc. (USCi) [63]. GeneSiC Semiconductor look to be the most advanced of these companies in terms of their product development, having had a 6.5 kV/80 A-rated thyristor device available for sampling as of November 2010. In [64], a 12 kV/1300 A 4H-SiC thyristor developed by Cree, Inc. has been shown to successfully operate using optical triggering of the gate, which is encouraging for future applications in the field of HVDC power transmission, where optically-triggered Si power devices are currently employed. USCi have also recently published their 4H-SiC 6.5 kV GTO thyristor efforts [65], which, with an active area of 4 mm^2, are capable of operating at 80 A peak current up to a maximum junction temperature of 175°C. This successful development has resulted in USCi attempting to up-scale their 4H-SiC GTO devices to the 15 kV range to offer further benefits for power transmission applications.

Next considering the current status of the development of 4H-SiC IGBT devices, it appears that Cree, Inc. have the most advanced IGBT technology, with the aforementioned competitors GeneSiC Semiconductor and USCi seemingly focussing on thyristor technology and not developing an IGBT device. A 2012 publication from Cree, Inc. [66]

has demonstrated both n- and p-channel 4H-SiC IGBTs, both capable of blocking in excess of 12 kV. The n-channel IGBT was found to have superior on-state characteristics, with a specific on-resistance of 5.3 mΩ-cm^2 at 200 A/cm^2 against 24 mΩ-cm^2 for the p-channel IGBT, though its blocking characteristics were found to be worse than the p-channel IGBT, blocking 12.5 kV against 15 kV for the p-channel device. However, the development of these high voltage 4H-SiC IGBT is an exciting step towards the realisation of future, more efficient SCC-VSC/MLC HVDC technology.

2.3.6 So, Why 4H-SiC?

On examination of Table 2.1, it is evident that both C and GaN generally have superior properties when compared to 4H-SiC, with the sole exception of GaN's thermal conductivity. As such, it is logical to question why 4H-SiC is favoured over these two materials for high voltage power electronics. Firstly, addressing the status of C semiconductor technology, it is apparent that the manufacture of conventional power devices in C is infeasible, due to the difficulty of doping the material to form n- and p-type device regions [67]. Furthermore, the wide band gap (5.5 eV) of C means that the formation of ohmic contacts is generally problematic. This wide band gap energy also means that the *pn* junction voltage is correspondingly higher than 4H-SiC; this means that this disadvantage needs to be offset by a lower voltage drop across the drift region of the device, which in turn means that C is only practical for blocking very high voltages, beyond the applications being targeted by the devices developed in this thesis. It is for these reasons that despite its excellent electrical and thermal properties, the use of C for power semiconductor devices is less attractive than 4H-SiC.

In recent years, research activity into the use of GaN for power electronics has seen a considerable increase, as a result of advances in the epitaxial growth of GaN layers [68]. However, bulk GaN substrates are hampered by very high defect densities and are only available in small diameters (currently 50 mm). Furthermore, the cost of bulk GaN is very high, of the order €100 per cm^2 [68]. As such, the use of a different material substrate onto which GaN is epitaxially grown is required, with typical substrate materials including Si, SiC and sapphire. However, this heteroepitaxy process prevents the fabrication of vertical structure power devices. Because of this, research into GaN power devices is predominantly focussed on lateral type devices, targeting blocking voltages typically less than 2 kV. Also, crucially for high voltage devices, GaN is a direct band gap semiconductor and thus has a very short carrier lifetime; this means that bipolar devices are not feasible in GaN, and hence GaN is not suitable for high voltage power electronics applications.

2.4 Summary

The aim of this Chapter was to introduce the high voltage power systems that are relevant to the work in this thesis, as well as provide an insight into the expected future trends of this particular application area, and the importance of power electronics in these systems. Following this, SiC was introduced, highlighting both its advantageous material properties for high voltage applications, in addition to some of the material problems that still exist, despite the significant progress made in recent years. Next, a review of the current status of 4H-SiC devices was given, which illustrated the recent technological advances that have lead to the commercial release of 4H-SiC MOSFETs and SBDs, as well as the current state-of-the-art in bipolar devices. Finally, a brief discussion of why 4H-SiC is the wide band gap material of choice for high voltage power electronics was outlined. The bipolar

PiN diode device, which is central to this thesis, has not been reviewed in this Chapter, a detailed review of the current state-of-the-art of this technology is given in the next Chapter.

Chapter 3

High Voltage 4H-SiC PiN Diode Technical Discussion

In this Chapter, the theoretical concepts that apply to the design of PiN diodes are introduced; these concepts will subsequently be applied in the following Chapters. Firstly, the fundamental operating principles of these devices that need to be understood when designing and optimising device structures are outlined. Following this, a discussion of high voltage junction termination is given, this being a key area of design for the devices that have been developed in this thesis. A second key area of the design and fabrication of these devices is the enhancement of the typically-low carrier lifetime in 4H-SiC material; as such, the mechanisms behind this low lifetime are discussed, as are methods that can be applied to improve this aspect of device performance. This is followed by a discussion of the fabrication issues that are encountered in the development of 4H-SiC power semiconductor devices. Finally, a review of the current status of high voltage 4H-SiC PiN diodes is given.

The discussion in this Chapter, and also the subsequent Chapters, presumes a level of understanding of basic semiconductor physics. This background theory is included in Appendix A.

3.1 PiN Diode Operating Principles

The PiN diode is one of most important power semiconductor devices for high voltage applications that are beyond the practical limits of unipolar-type SBDs, as discussed in Section 2.2.1. The structure typically consists of a lightly-doped middle region (the drift region) which is sandwiched by a heavily doped $N+$ region (the cathode) at one end and a heavily doped $P+$ region (the anode) at the other end (also referred to as 'emitters'), as illustrated in Figure 3.1. When the device is in the on-state, holes are injected from the positively-biased $P+$ anode and electrons are injected from the negatively-biased $N+$ cathode into the drift region. Referred to as conductivity modulation, this serves to reduce the resistance of the drift region, thus reducing on-state power dissipation. Conversely, when the cathode is positively-biased with respect to the anode, the injected carriers are swept out of the drift region, eventually forming a depletion region which allows the diode to block high reverse voltages. This depletion region cannot fully form until all the the carriers are removed from the drift region; as such, the transient characteristics of the PiN diode, particularly at turn-off, are poor when compared to the SBD, and represent the cost paid for low on-state losses at high blocking voltages.

3.1.1 Forward Conduction

In this section, the physics that govern the on-state behaviour of PiN diodes are discussed. As the devices that are being designed in this work are intended to be operated under high-level injection conditions, the discussion will be limited to this mode of operation.

When the on-state voltage drop of the PiN diode increases, the injected minority carrier concentration also increases, according to the "Law of the Junction", which is

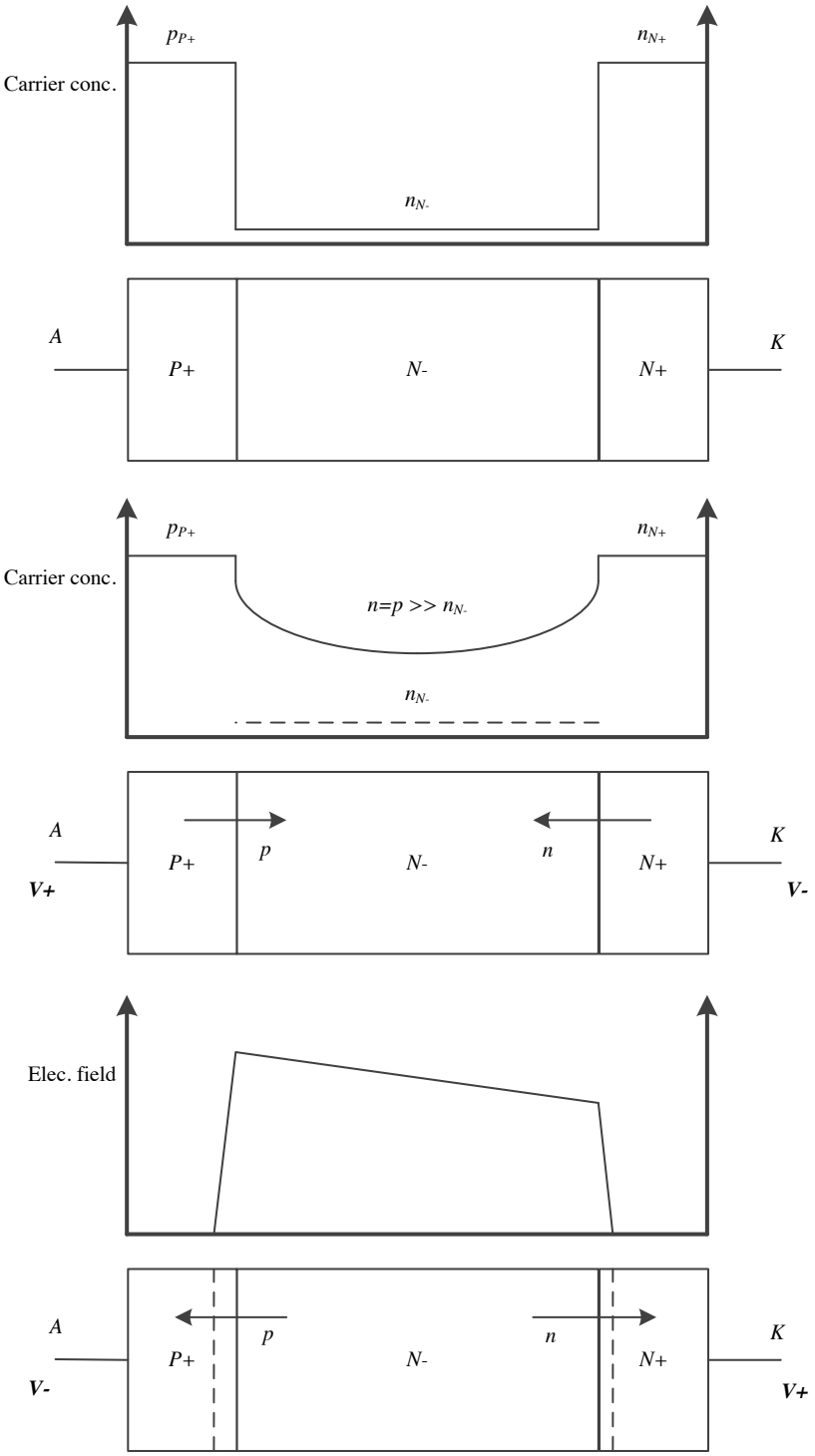


Figure 3.1: The PiN diode at zero bias (top), under forward bias (middle) and reverse bias (bottom).

derived under Boltzmann's quasi-equilibrium assumptions and is given by

$$p_N(0) = p_{0N} e^{qV_a/kT} \tag{3.1}$$

where p_{0N} is the hole concentration in equilibrium on the N-side of the junction. Eventually, the minority carrier concentration will exceed the background doping concentration (N_D) in the drift region, referred to as high-level injection. Under this condition, charge neutrality requires that the concentrations of electrons and holes in the drift region becomes equal, or $p(x) = n(x)$. This increase in injected carriers serves to reduce the background resistance of the drift region, and, assuming unity injection efficiency, $\gamma = 1$, for both the $P+$ and $N+$ emitters, a first order approximation, which states that the forward current density J_F is determined by carrier recombination in the drift region, can be made

$$J_F = \frac{2qdp^*}{\tau_{HL}} \tag{3.2}$$

where d is half of the drift region width, and τ_{HL} is the high-level carrier lifetime (which is the carrier lifetime in the drift region under high-level injection conditions). The approximation of a uniform carrier distribution in the drift region is here denoted p^* (though n^* could be equally applied). Although Equation 3.2 is a simplification of a complex conduction mechanism (discussed below), it enables qualitative prediction of the performance tradeoffs associated with the PiN diode. A key observation here is that an increase in carriers in the drift region corresponds to an increase in the forward current density J_F. This in turn implies that J_F has little effect on the voltage dropped across the drift region of the device, as the resistance of the drift region decreases with increasing charge. A second observation that is made is that the charge stored in the drift region is directly proportional to the high-level lifetime. As such, in order to obtain a higher carrier con-

centration in the drift region and thus lower on-resistance, a longer lifetime and more switching losses are required.

In order to confirm the previously mentioned qualitative observations, a more detailed analysis of the carrier profile in the PiN diode is required. In order to solve this, we start with the steady-state continuity equation under high-level injection conditions

$$D_a \frac{d^2 p(x)}{dx^2} - \frac{p(x)}{\tau_{HL}} = 0 \tag{3.3}$$

where D_a is the ambipolar diffusion constant. Meanwhile, using each end of the drift region as boundary conditions denoted by $-d$ and $+d$ for the $P+$ and the $N+$ end respectively, the current density can be written as

$$J = Jp_{x=-d} = q\mu_p p_{x=-d}\mathscr{E}_{x=-d} + qD_p \left.\frac{dp(x)}{dx}\right|_{x=-d} = 2qD_p \left.\frac{dp(x)}{dx}\right|_{x=-d} \tag{3.4}$$

$$J = Jn_{x=+d} = q\mu_n n_{x=+d}\mathscr{E}_{x=+d} + qD_n \left.\frac{dn(x)}{dx}\right|_{x=+d} = 2qD_n \left.\frac{dn(x)}{dx}\right|_{x=+d} \tag{3.5}$$

where D_n and D_p are the electron and hole diffusion constants respectively. Also, when $\gamma = 1$, it can be stated that

$$Jn_{x=-d} = Jp_{x=+d} = 0 \tag{3.6}$$

and $p = n \gg n_{n0}, p_{n0}$ in the drift region. Based on the boundary conditions outlined in Equations 3.4 and 3.5, Equation 3.3 can be solved to give the carrier concentration throughout the drift region as in [69]

$$n(x) = p(x) = \frac{\tau_{HL} J}{2qL_a}\left[\frac{\cosh(x/L_a)}{\sinh(d/L_a)} - B\frac{\sinh(x/L_a)}{\cosh(d/L_a)}\right] \tag{3.7}$$

where L_a is the ambipolar diffusion length, given by

$$L_a = (D_a \tau_{HL})^{0.5} \tag{3.8}$$

and B is the mobility asymmetry factor, given by

$$B = \frac{\mu_n - \mu_p}{\mu_n + \mu_p} \tag{3.9}$$

In 4H-SiC, the mobility asymmetry factor is $B \approx 0.8$, which is markedly more asymmetric than for Si, where $B \approx 0.5$. The result of this is a large charge build up near the $P+/N-$ junction in 4H-SiC PiN diodes under forward bias when compared to similar Si devices. This large build up of charge can result in poor on-state versus switching loss tradeoffs, due to the fact that more charge is required to ensure adequate conductivity modulation across the whole of the drift region. The calculated charge distribution of a Si and a 4H-SiC PiN diode is illustrated in Figure 3.2.

Once the carrier concentration in the drift region has been found, Equations 3.4, 3.5 and 3.6 can be used to determine the position-dependent electric field

$$\mathscr{E}(x) = \frac{J_F}{q(\mu_n + \mu_p)n} - \frac{kT}{q}\frac{B}{n}\frac{dn(x)}{dx} \tag{3.10}$$

Here, the first term is due to the ohmic drop in the drift region whilst the second term is associated with the asymmetry in the carrier mobility. By integrating Equation 3.10 over its width, the forward voltage drop of the modulated drift region, V_M, can be found

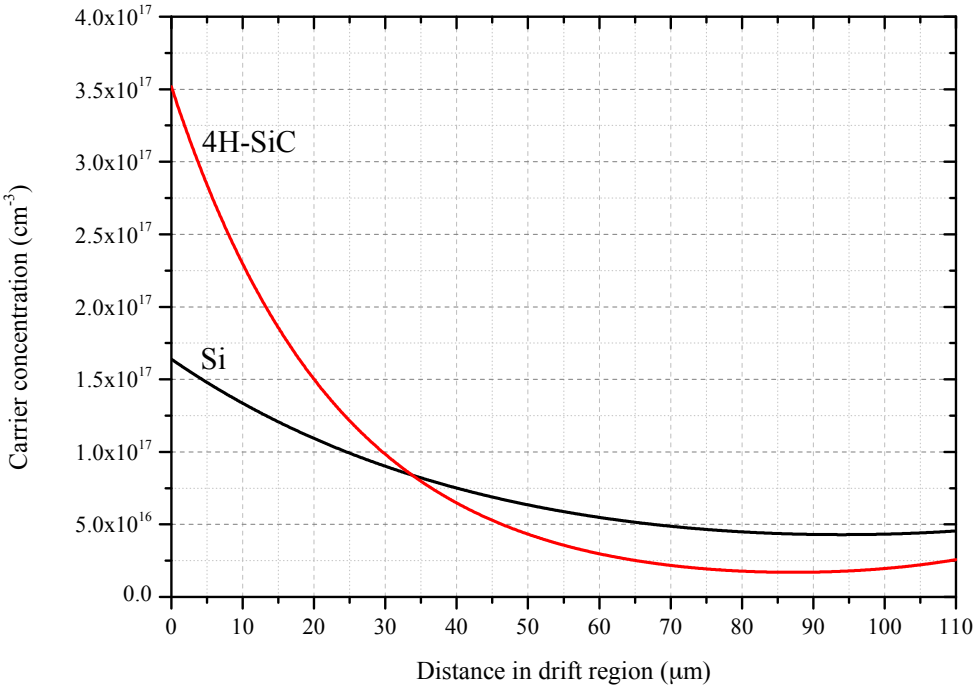


Figure 3.2: Calculated charge distribution in Si and 4H-SiC PiN diodes with identical drift region design (W_D=110 μm, γ=1, J_F=100 A/cm^2, τ_{HL}=1 μs).

$$\frac{V_M}{kT/q} = \left[\frac{8b}{(b+1)^2}\frac{\sinh(d/L_a)}{\sqrt{1-B^2\tanh^2(d/L_a)}}\arctan\left[\sqrt{1-B^2\tanh^2(d/L_a)}\sinh(d/L_a)\right]\right] + B\ln\left[\frac{1+B^2\tanh^2(d/L_a)}{1-B^2\tanh^2(d/L_a)}\right] \tag{3.11}$$

where b is given by

$$b = \frac{\mu_n}{\mu_p} \tag{3.12}$$

Equation 3.11 is plotted as a function of d/L_a for both 4H-SiC and Si in Figure 3.3. As

outlined in [69], this complex expression can be approximated by

$$V_M \approx \frac{2kT}{q}\left(\frac{d}{L_a}\right)^2 \tag{3.13}$$

for d/L_a ratios less than 2. For d/L_a ratios greater than 2, the approximation is

$$V_M \approx \frac{3\pi kT}{8q}\mathrm{e}^{d/L_a} \tag{3.14}$$

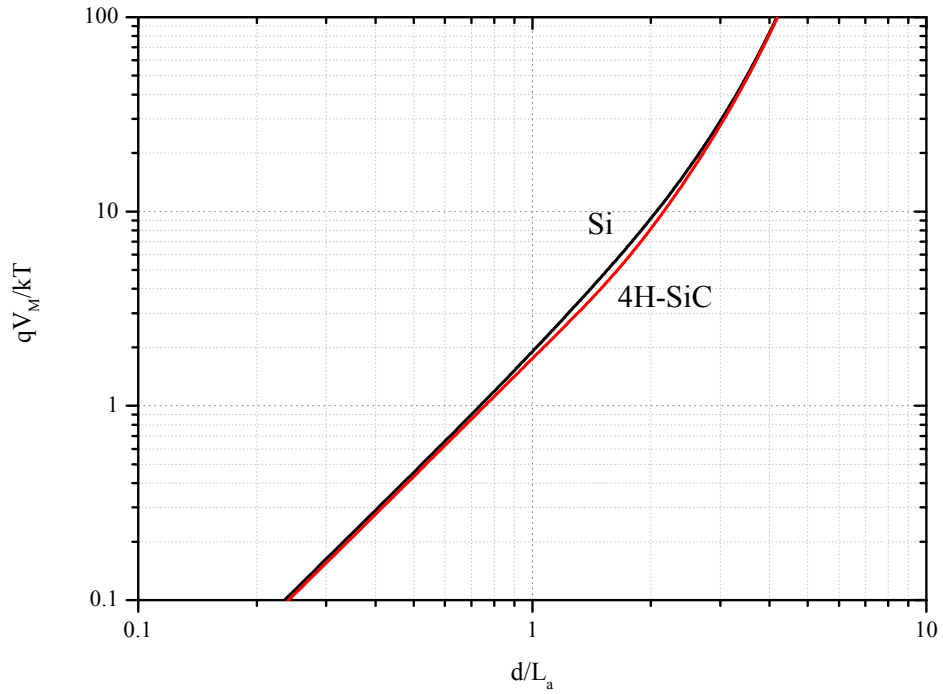


Figure 3.3: Drift region voltage drop as a function of d/L_a for Si and 4H-SiC PiN diodes.

The previously given equations for V_M only concern the forward voltage drop across the modulated drift region of the PiN diode. In order to find the total on-state voltage drop V_F of the device, the drops across the $P+$ and $N+$ emitters must be included, such

that

$$V_F = V_M + V_{P+} + V_{N+} \tag{3.15}$$

Based on the law of the junction, the electron and hole concentrations at both ends of the drift region can be related to their equilibrium values

$$p_{nx=-d} = \frac{n_i^2}{N_D^+} e^{\frac{qV_{P+}}{kT}} \tag{3.16}$$

and

$$n_{nx=+d} = N_D^+ e^{\frac{qV_{N+}}{kT}} \tag{3.17}$$

where N_D^+ is the ionised dopant concentration in the drift region. Because $p(x) = n(x)$ under high-level injection conditions, the sum of the two emitter voltage drops can be written as

$$V_{P+} + V_{N+} = \frac{kT}{q} \ln \left[\frac{n_{x=-d} n_{x=+d}}{n_i^2} \right] \tag{3.18}$$

By combining Equation 3.7 with Equations 3.15 and 3.18, the forward J-V characteristics of the PiN diode can be expressed as

$$J_F = \frac{2qD_a n_i}{d} F\left(\frac{d}{L_a}\right) e^{\frac{qV_A}{2kT}} \tag{3.19}$$

where

$$F\left(\frac{d}{L_a}\right) = \left[\frac{d}{L_a} \tanh\left(\frac{d}{L_a}\right)\right] \left[1 - B^2 \tanh^4\left(\frac{d}{L_a}\right)\right]^{-\frac{1}{2}} e^{\frac{-qV_M}{2kT}} \tag{3.20}$$

Equation 3.20 is illustrated in Figure 3.4, again for both 4H-SiC and Si. From Equation 3.19 and Figure 3.4 it can be seen that the ambipolar diffusion length needs to be around half the drift region width in order to minimise the forward voltage drop of the PiN diode. It can also be seen from Equation 3.19 that when written in the form of the ideal diode

equation, the ideality factor $\eta = 2$ indicates high-level injection conditions.

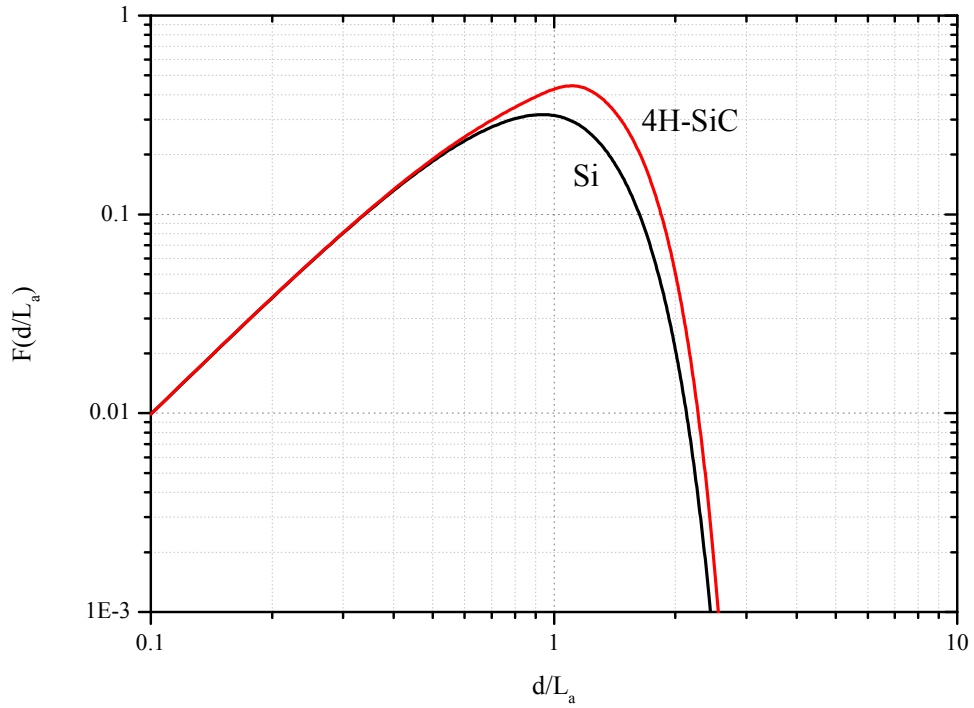


Figure 3.4: F(d/L_a) plotted for Si and 4H-SiC PiN diodes.

It is important to note that the current-voltage characteristics that have been outlined above do not account for higher-order effects that impact semiconductor devices when operated at high current densities, for example the decrease in carrier mobility due to carrier-carrier scattering, auger recombination and injection efficiency reduction. These effects are included in the numerical simulation models used for the design of the high voltage 4H-SiC PiN diodes in this work, discussed in Section 4.1.

Under high-level injection conditions, and neglecting radiative recombination and surface effects, the effective carrier lifetime within the drift region of the PiN diode is typically modelled by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{HL}} + \frac{1}{\tau_{Auger}} \tag{3.21}$$

where τ_{HL} is the high-level Shockley-Read-Hall (SRH) lifetime and τ_{Auger} is the Auger recombination governed lifetime. However, the carrier concentration also has an impact on the auger lifetime component; the relationship given by

$$\tau_{Auger} = \frac{1}{\gamma_3 n^2} \tag{3.22}$$

where γ_3 is the Auger recombination coefficient and n is the carrier concentration. If operating conditions are such that Auger recombination in the drift region is the dominant recombination process (typically when the injected carrier concentration is greater than 10^{17} cm^{-3}), Equation 3.2 can be modified such that

$$J_F = 2qd\gamma_3 n^3 \tag{3.23}$$

It can therefore be seen that under high-level injection conditions when Auger recombination dominates in the drift region, the relationship between forward current and stored charge in the drift region of the PiN diode becomes sub-linear. This means that the voltage drop across the drift region is no longer independent of the operating current, and the device exhibits larger on-state losses.

Up to now, the analysis of the forward conduction behaviour of the PiN diode has assumed that the injection efficiency, γ, of the two emitter-drift region junctions is equal to unity. However, though this is a safe assumption to make at low forward biases, at high current densities this parameter can govern the conduction behaviour of conventional 4H-SiC PiN diodes. The effects of emitter recombination on the forward conduction of the PiN diode can be described by representing the electron current density in the $P+$

emitter as

$$Jn_{P+} = J_{ns}e^{\frac{qV_{P+}}{kT}} \tag{3.24}$$

and representing the hole current density in the $N+$ emitter as

$$Jp_{N+} = J_{ps}e^{\frac{qV_{N+}}{kT}} \tag{3.25}$$

where J_{ns} and J_{ps} are the saturation current densities for the $P+$ and $N+$ emitters, respectively, and are expressed as

$$J_{ns} = \frac{qD_{n,P+}n_{p0}}{L_{n,P+}\tanh(W_{P+}/L_{n,P+})} \tag{3.26}$$

and

$$J_{ps} = \frac{qD_{p,N+}p_{n0}}{L_{p,N+}\tanh(W_{N+}/L_{p,N+})} \tag{3.27}$$

Under quasi-equilibrium conditions, the injected carrier concentrations on either side of the $P+/N-$ junction are related by

$$p_p n_p = n_n p_n \tag{3.28}$$

From Equation 3.1, and noting that $p_P = p_{P0}$, combining with Equations 3.24 and 3.25 means it can be stated that

$$n_n n_p = n_n^2 = p_n^2 = p_{p0}n_{p0}e^{\frac{qV_{P+}}{kT}} = n_i^2 e^{\frac{qV_{P+}}{kT}} \tag{3.29}$$

in the drift region under high-injection conditions, and the electron and hole current

densities in the $P+$ and $N+$ emitters can be written as

$$Jn_{P+} = J_{ns}\left(\frac{p_{Nx=-d}}{n_i}\right)^2 \tag{3.30}$$

$$Jp_{N+} = J_{ps}\left(\frac{p_{Nx=+d}}{n_i}\right)^2 \tag{3.31}$$

Finally, the total forward current density can be described as

$$J_F = Jn_{P+} + Jp_{N+} + J \tag{3.32}$$

where J is the current due to recombination in the drift region. It can therefore be seen that if the emitter injection efficiencies are reduced (maximising Jn_{P+} and Jp_{N+} while minimising J), Equations 3.30, 3.31 and 3.32 state that there is a square root dependence of stored charge in the drift region on J_F, as opposed to a linear dependence. Though this can result in an increased forward voltage drop across the PiN diode, careful design of the emitter regions can be useful in improving the switching performance of the device.

3.1.2 Reverse Blocking

In order to block high reverse voltages, PiN diodes require thick, lightly doped drift regions. By employing conductivity modulation as described in the previous Section, a low on-state voltage drop across this normally-resistive region can be realised, so long as the carrier lifetimes in the material are sufficiently long. Because low carrier lifetimes in 4H-SiC can be a problem for high voltage PiN diodes and result in a high on-state voltage drop due to insufficient conductivity modulation, it is advantageous to utilise a 'punch-through' structure, described below, which allows a thinner drift region for a given

reverse blocking voltage.

When a reverse bias is applied to a PiN diode, the drift region is depleted of carriers, starting from the $P+/N-$ junction and extending towards the $N-/N+$ junction. Because the drift region is lightly doped, the depletion region is able to reach the $N+$ emitter, often at fairly low reverse bias. The electric field profile associated with this scenario is illustrated in Figure 3.5, and is related to the voltage across the PiN diode by

$$V_R = \int_0^{W_d} \mathscr{E}(x)dx \tag{3.33}$$

where V_R is the reverse bias voltage. In addition, the electric field at each end of the drift region (assuming finite doping) are related by

$$\mathscr{E}_{x=-d} - \mathscr{E}_{x=+d} = \frac{2qdN_D}{\varepsilon_S} \tag{3.34}$$

where N_D is the dopant concentration in the drift region and ε_S is the static dielectric constant of semiconductor material.

Briefly touched on in Chapter 2 was the impact ionisation process, whereby, due to high electric fields in the device depletion region caused by large reverse bias voltages, carriers gain sufficient kinetic energy to create electron-hole pairs as a result of collisions with lattice atoms. This is a multiplicative process, as the carriers that are generated themselves gain sufficient energy to create further electron-hole pairs. Once the rate of this process tends to infinity, avalanche breakdown of the semiconductor is reached. The maximum electric field, and hence reverse blocking voltage, of a junction is dictated by the impact ionisation rates, α_n and α_p, which are defined as the number of electron-hole pairs generated per carrier (electrons and holes respectively), per centimetre traversed

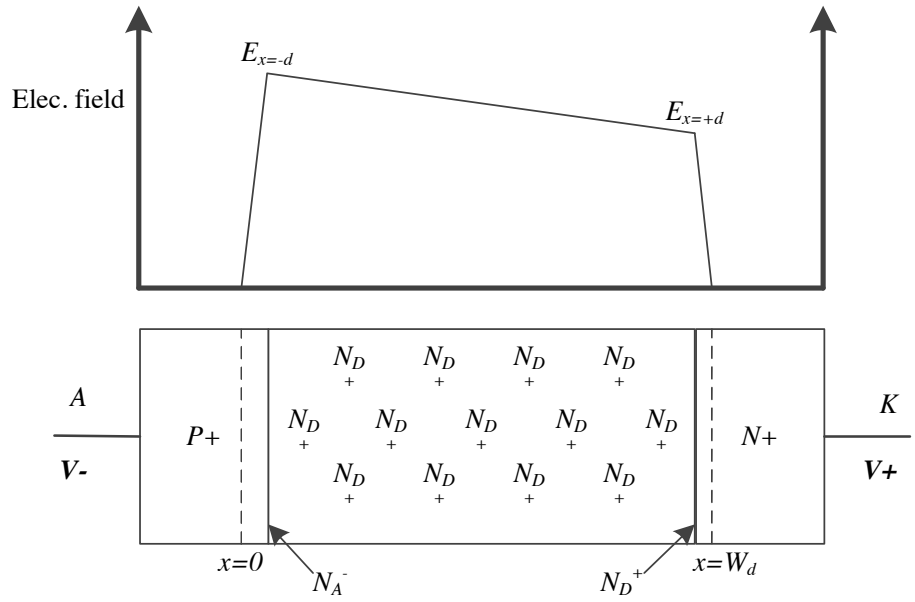


Figure 3.5: One-dimensional approximation of the electric field distribution of the PiN diode under reverse bias.

in the direction of the applied electric field. These impact ionisation coefficients can be modelled by

$$\alpha_n = a_n \exp\left(\frac{-b_n}{\mathscr{E}}\right)^{cn} \tag{3.35}$$

for n-type material, and

$$\alpha_p = a_p \exp\left(\frac{-b_p}{\mathscr{E}}\right)^{cp} \tag{3.36}$$

for p-type material, where $a_{n,p}$, $b_{n,p}$ and $c_{n,p}$ are material-dependent parameters, and $\mathscr{E}$ is the electric field. The onset of avalanche breakdown occurs when the multiplication of carriers in the depletion region at high fields tends to infinity, which can be represented by

$$M(x) = \frac{\exp\left[\int_0^x (\alpha_n - \alpha_p) dx\right]}{1 - \int_0^{W_d} \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p) dx\right] dx} \tag{3.37}$$

Therefore, when the following condition is satisfied

$$\int_0^{W_d} \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p) dx\right] dx = 1 \tag{3.38}$$

carrier generation has reached infinity and junction breakdown occurs. At this point, the electric field value is referred to as the critical electric field, $\mathscr{E}_C$, therefore, for a PiN diode with a punch-through structure $\mathscr{E}_{x=-d} = \mathscr{E}_C$ at breakdown. Equation 3.34 can now be redefined as

$$\mathscr{E}_{x=+d} = \mathscr{E}_C - \frac{2qdN_D}{\varepsilon_S} \tag{3.39}$$

Based on the assumption that the drift region supports all of the applied voltage, the breakdown voltage of the punch-through PiN diode is given by evaluating Equation 3.33 as

$$BV_{PT} = 2d\mathscr{E}_C - \frac{4qd^2N_D}{\varepsilon_S} \tag{3.40}$$

The doping concentration of the semiconductor also has an effect on the critical electrical field, and thus the breakdown voltage of the device, as outlined in [69], where the relationships are given by

$$\mathscr{E}_C(\text{Si}) = 4.01 \times 10^3 N_D^{1/8} \tag{3.41}$$

for Si, and

$$\mathscr{E}_C(\text{4H-SiC}) = 3.3 \times 10^4 N_D^{1/8} \tag{3.42}$$

for 4H-SiC.

Prior to the onset of avalanche breakdown in the PiN diode, the reverse leakage current that flows through the device is theoretically governed by two main processes. The first process is electron-hole generation within the depletion region, from which the generation

leakage current can be determined by

$$J_G = \frac{-qn_iW_d}{2\tau_{SC}} \tag{3.43}$$

where τ_{SC} is the carrier generation lifetime in the depletion region and W_d is the width of the depletion region. As such, the leakage current that arises from carrier generation in the depletion region will increase by a square root with the applied reverse bias as the depletion region width expands until the onset of punch-through. In addition to the generation current described by Equation 3.43, surface generation also forms part of the total leakage current in the PiN diode. By adding a surface generation term to the generation lifetime, this can be described by

$$J_G = \frac{-qn_iW_d}{2\tau_{g,eff}} = \frac{qn_iW_d}{2}\left[\frac{1}{\tau_{SC}} + S\frac{P}{A}\right] \tag{3.44}$$

where S is the surface generation velocity, P is the perimeter of the depletion width edge on the surface of the device, and A is the area of the depleted surface.

The second process that contributes to the reverse leakage current of the PiN diode is the diffusion current that arises from minority carriers generated in the neutral emitters close to the depletion region boundaries. This diffusion current is represented by

$$J_{Diff} = \frac{qD_p p_{0N+}}{L_p} + \frac{qD_n n_{0P+}}{L_n} \tag{3.45}$$

where L_p and L_n are the minority carrier diffusion lengths for holes and electrons in the emitters. Other than for very low reverse biases, this diffusion current is independent of the applied reverse voltage, though is strongly dependent on temperature, as p_{0N+} and n_{0P+} increase by n_i^2.

3.1.3 Reverse Recovery Behaviour

The use of conductivity modulation means that the PiN diode is capable of low on-state losses compared to unipolar-type devices of equivalent high blocking voltage. However, it is this mechanism that is also the cause of the principle disadvantage of the PiN diode, namely the transient characteristics of the device. Due to the physical operation of the PiN diode, slow turn-on and turn-off transients are an inherent characteristic of the device. When a PiN diode is switched from the reverse blocking state to the on-state, the injected carriers take a finite amount of time to traverse the drift region, meaning that this high-resistance region is unmodulated for some time. As such, the PiN diode can exhibit a large forward voltage drop immediately after a forward bias pulse is applied. This forward voltage drop will gradually decrease as the charge builds up in the drift region, eventually reaching its steady state value. However, even assuming no conductivity modulation and thus the drift region resistance given by

$$R_D = \frac{W_D}{q\mu_n N_D A} \tag{3.46}$$

the voltage drop of a typical 10 kV-rated 4H-SiC PiN diode (with $W_D = 110$ μm and $N_D = 6 \times 10^{14}$ cm^{-3}) is approximately 13 V at 100 A/cm^2, which is significantly less than the rated blocking voltage. As such, the forward recovery power dissipation is typically much lower than the power dissipation arising from reverse recovery.

When the PiN diode is switched from the on-state to the reverse blocking state, the charge that is stored in the drift region must be extracted before the device can support a reverse voltage in the off-state. The injected carriers are swept out of the drift region and depletion layers form at the $P+/N-$ and $N-/N+$ junctions, eventually merging once all of the charge has been removed. During the finite time prior to all of the charge

being removed from the drift region, a reverse current flows; this is due to a negative applied voltage which appears across external inductance because the diode cannot yet support a reverse voltage. The reverse voltage only begins to build up once the depletion layers appear, which is after the reverse current has begun flowing. As such, there is a period of time during which both the current and voltage are large and negative, thus resulting in large power dissipation during reverse recovery. This can impose limitations on the maximum switching frequency of the device, and necessitate derating the device operating current. Furthermore, overall circuit switching speeds can be constrained as a result of a long diode recovery time, t_{rr}.

Illustrated in Figure 3.6 are the PiN diode reverse recovery waveforms when switched off with an inductive load. As shown in this Figure, the reverse recovery current is modelled with a triangular waveform [69]. In power electronics circuits, inductive switching is the most common switching condition for rectifiers such as PiN diodes. The presence of an inductive load means that the turn-off current slew rate, or di/dt, is constant, due to the full reverse voltage being applied across the inductor prior to the PiN diode being capable of blocking. The current slew rate, referred to as a in Figure 3.6, is governed by the circuit parameters as given by

$$a = \frac{di}{dt} \approx \frac{V_R}{L} \tag{3.47}$$

based on the assumption that the reverse clamping voltage V_R is much larger than the forward voltage drop V_F of the diode.

The reverse recovery characteristics that result are governed by the charge that is stored in the drift region of the PiN diode. Figure 3.7 shows the charge profile in the drift region at selected intervals during the switching of an inductive load, corresponding

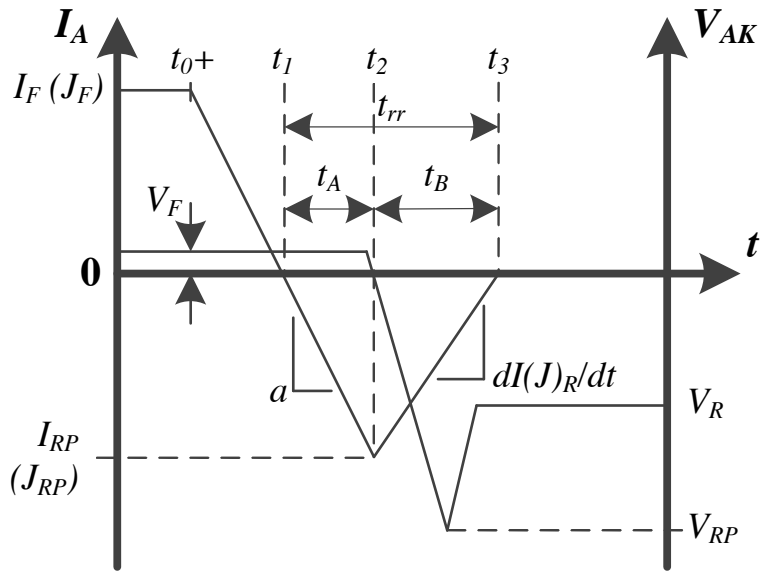


Figure 3.6: Reverse recovery approximation waveforms with inductive load switching.

with the times indicated on Figure 3.6. Also shown in this Figure is the corresponding one-dimensional electric field distribution in the drift region. Prior to turn-off, $t = 0$, the catenary shape charge profile described by Equation 3.7 is exhibited. At time $t = t_0+$, a reverse bias voltage is applied to the diode; at this point the charge in the drift region of the device begins to be swept out and the recovery process begins. Next, at time $t = t_1$, the polarity of the current flowing through the diode changes, and the diode begins to conduct reverse current. As shown in Figure 3.7, the zero-crossing of the current occurs when the gradient of the charge profile reaches zero at the boundaries of the drift region ($x = -d$ and $x = +d$).

After time $t = t_1$, the reverse current continues to increase as governed by the constant a until the diode is able to support some of the reverse voltage at time $t = t_2$. As indicated in Figure 3.7, this peak reverse current I_{RP} (or J_{RP}) occurs when the carrier concentration at the $P+/N-$ junction reaches zero, therefore allowing a depletion layer to form. It is

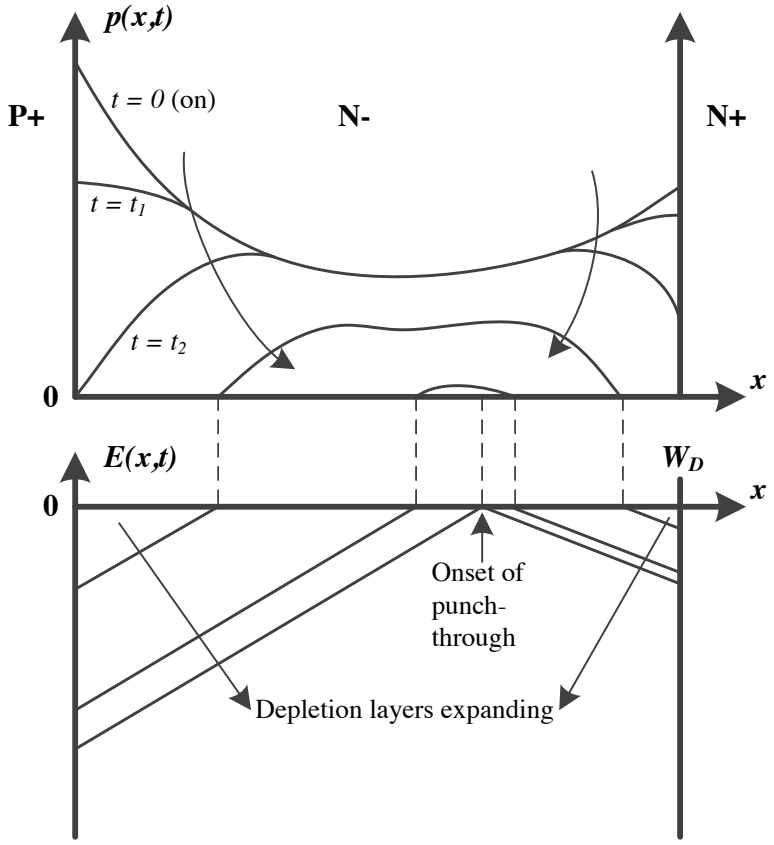


Figure 3.7: Carrier storage region profile and corresponding 1-D electric field distribution during reverse recovery.

found that the reverse peak current density is proportional to the gradient of the charge profile at the $P+/N-$ junction; as such, a build up of charge at this junction of a PiN diode can cause larger reverse peak current densities and hence increase switching losses of the device. As discussed in Section 3.1.1, 4H-SiC has a relative high mobility asymmetry factor when compared to Si, meaning that this problem is particularly detrimental to the switching performance of 4H-SiC PiN diodes. However, techniques such as the tailoring of emitter injection efficiency and localised lifetime control can be employed to reduce the charge build up near the $P+/N-$ junction and hence improve the reverse recovery

characteristics of PiN diodes.

The first phase of the PiN diode reverse recovery, referred to as t_A in Figure 3.6, is the time during which charge is removed from the drift region prior to the diode blocking any of the reverse voltage. After time $t = t_2$, the second phase of the diode recovery, denoted t_B, occurs; during this time the remaining charge is removed from the drift region until it is totally devoid of any electron-hole plasma. This causes the reverse current through the diode to decrease whilst the reverse voltage across the device increases until the recovery process is complete and the diode is in the reverse blocking state. This can be inferred from Figure 3.7, as the gradient of the charge profile gradually decreases as the charge is removed from the drift region.

A key parameter of PiN diode reverse recovery is the "softness factor", S, which is defined as the ratio of the recovery phases, t_B/t_A. As discussed in [69], the rate of change in the reverse recovery current during the t_B phase can be high ($S < 1$), resulting in high, potentially destructive, transient voltages across stray inductances in the diode circuit path. This undesirable effect is referred to as "snappy recovery", and can be mitigated by reducing the charge build-up at the $P+/N-$ junction, thus allowing the depletion layer to form soon after the reverse recovery process begins, i.e. t_A is reduced. However, as observed by Bartsch et al. [70], a build up of charge at the $N-/N+$ junction can result in significant dI_R/dt under hard switching conditions, in devices where the charge near the $P+/N-$ junction is low. As such, the stored charge profile in the drift region should be made symmetrical in order to achieve soft recovery characteristics.

Based on Figure 3.6, the total power dissipation of the PiN diode during reverse

recovery can be described as

$$\begin{aligned} P_{D,rr} &= f_{SW}\int_{t_0+}^{t_1}|V(t)||I(t)|dt + f_{SW}\int_{t_1}^{t_2}|V(t)||I(t)|dt + f_{SW}\int_{t_2}^{t_3}|V(t)||I(t)|dt \\ &= P_0 + P_A + P_B \end{aligned} \tag{3.48}$$

During the reverse recovery process it is found that the majority of the power dissipated occurs during the second phase of the recovery (t_B), when the diode is conducting reverse current whilst simultaneously supporting an increasing reverse voltage. It is therefore evident that whilst a relatively large t_B (with respect to t_A) is favourable for achieving soft reverse recovery characteristics and minimising transient voltage spikes, it can also result in a higher total power dissipation for the device.

In terms of quantifying the turn-off switching performance of the PiN diode, the charge removed during the turn-off transient, or Q_{rr}, is probably the most important reverse recovery parameter, and can be determined by integrating the reverse recovery current waveform. This is given by

$$Q_{rr} = \int_{t_1}^{t_3} J(t)dt \tag{3.49}$$

With reference to Figure 3.7, Q_{rr} can be represented by the integrated charge profile in the drift region at time $t = t_1$, thus

$$Q_{rr} = q\int_{-d}^{+d} n(x)dx \tag{3.50}$$

From the above analysis, it is evident that the stored charge in the drift region of the PiN diode should be minimised in order to improve the switching performance of the device. By reducing Q_{rr}, the reverse recovery power dissipation $P_{D,rr}$, the peak

reverse current I_{RP} and the reverse recovery time t_{rr} are all reduced. Furthermore, by tailoring the charge profile in the drift region, softer reverse recovery characteristics can be achieved, a more optimised on-state versus switching loss trade-off can be realised, and reverse peak current densities can be reduced. As the development of high voltage PiN diodes has evolved, a variety of methods to modify both the total charge and the charge profile within the device have been successfully employed to optimise the on-state versus switching loss trade-off.

As can be inferred from Equation 3.7, by reducing the carrier lifetime in the drift region the profile of the stored charge in the PiN diode can be modified. In practice, this is achieved by the diffusion of gold (Au) or platinum (Pt) (in Si devices), or by electron irradiation [71], which serve to introduce deep level recombination centres within the energy band gap. Moreover, localised lifetime reduction can also be employed to reduce the build up of charge near the $P+/N-$ and $N-/N+$ junctions [72,73]. However, though this technology has matured for Si devices, this is not yet the case for 4H-SiC devices. A simpler method for optimising the switching performance of PiN diodes is to use emitter injection efficiency control; this has been successfully demonstrated by Losee et al. [74] for high voltage 4H-SiC PiN diodes.

3.2 High Voltage Junction Termination

Up to now, the reverse voltage blocking performance of PiN diodes has been based on the ideal one-dimensional impact ionisation properties of the semiconductor. However, in practice, two- and three-dimensional effects mean that specially designed edge termination structures and proper layout design rules are required to minimise electric field build up and achieve high blocking voltages in practice. Figure 3.8 shows the cross-section of

a cylindrical planar junction; this is the basis for the analysis of the two-dimensional junction breakdown. As outlined by Baliga and Ghandhi [75], Poisson's equation can be expanded to cylindrical coordinates as follows:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dV}{dr}\right) = -\frac{1}{r}\frac{d}{dr}(r\mathscr{E}) = -\frac{qN_D}{\varepsilon_S} \tag{3.51}$$

where the potential $V(r)$ and the electric field $\mathscr{E}(r)$ are defined along the radius vector r. Solving Equation 3.51 for the electric field within the depletion region gives

$$\mathscr{E}(r) = \frac{qN_D}{2\varepsilon_S}\left(\frac{r^2 - r_d^2}{r}\right) \tag{3.52}$$

and for the voltage distribution gives

$$V(r) = \frac{qN_D}{2\varepsilon_S}\left[\left(\frac{r^2 - r_J^2}{2}\right) + r_d^2 \ln\left(\frac{r}{r_J}\right)\right] \tag{3.53}$$

Because the radius of curvature of the metallurgical junction, r_J, is small in comparison with that of the depletion layer boundary r_d, the maximum electric field that is generated in the two-dimensional junction is much greater than that generated in the theoretical one-dimensional case. However, the electric field is even further enhanced when considering three-dimensional, or spherical, effects in device structures. In practice, a spherical junction would be formed at each of the four corners of a rectangular implant window, though by proper layout design the spherical junction problem can be reduced to that of the cylindrical junction. In a similar fashion to the two-dimensional case, Poisson's equation can be written in spherical coordinates [75]

$$\frac{1}{r^2}\frac{d}{dr}\left(r^2\frac{dV}{dr}\right) = -\frac{1}{r^2}\frac{d}{dr}(r^2 E) = -\frac{qN_D}{\varepsilon_S} \tag{3.54}$$

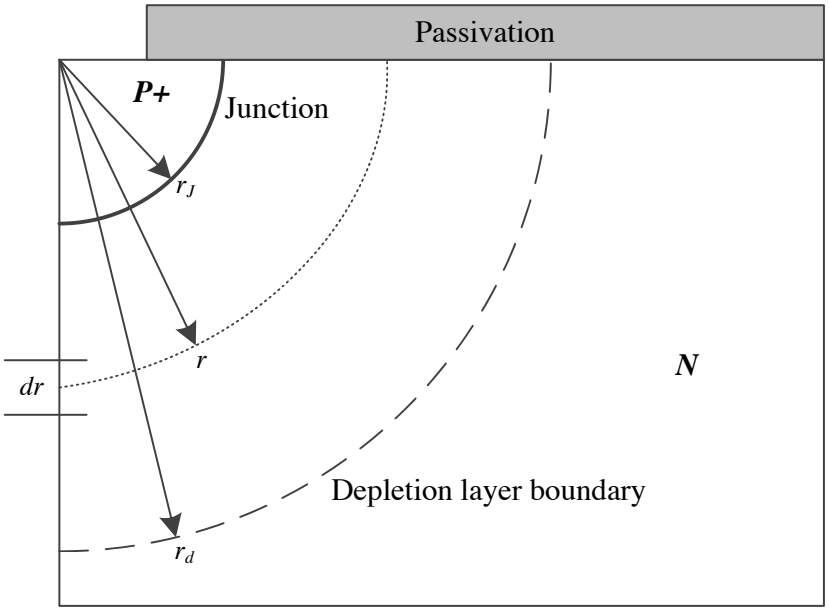


Figure 3.8: The two-dimensional (cylindrical) $P+/N-$ junction.

Solving for the electric field in the depletion region gives

$$\mathscr{E}(r) = \frac{qN_D}{3\varepsilon_S}\left(\frac{r^3 - r_d^3}{r^2}\right) \tag{3.55}$$

and for the voltage distribution gives

$$V(r) = \frac{qN_D}{3\varepsilon_S}\left[\left(\frac{r^2 - r_J^2}{2}\right) + r_d^3\left(\frac{1}{r} - \frac{1}{r_J}\right)\right] \tag{3.56}$$

It can be seen from Equations 3.52 and 3.55 that the electric field crowding at the edge of the metallurgical junction is made worse when the depletion region increases in width. In addition, due to the very low dopant diffusion coefficients and shallow implanted junction depths (typically less than 1 μm) in 4H-SiC, the design of high voltage devices that require thick ($\approx$100 μm) $N-$ layers is further complicated. The impact of cylindrical

and spherical breakdown on the blocking performance for 4H-SiC is illustrated in Figure 3.9. The impact of increasing the drift region width on the breakdown voltage capability of the device is evident; for a 1 kV PiN diode design that requires a drift region width of around 5 μm based on ideal parallel-plane conditions, a 1 μm deep $P+$ implanted region would yield a cylindrical breakdown of approximately 45% of the ideal value, assuming no edge termination structures were used. If the device is scaled up to block 10 kV, the expected cylindrical breakdown is now approximately just 10% of the ideal parallel-plane value.

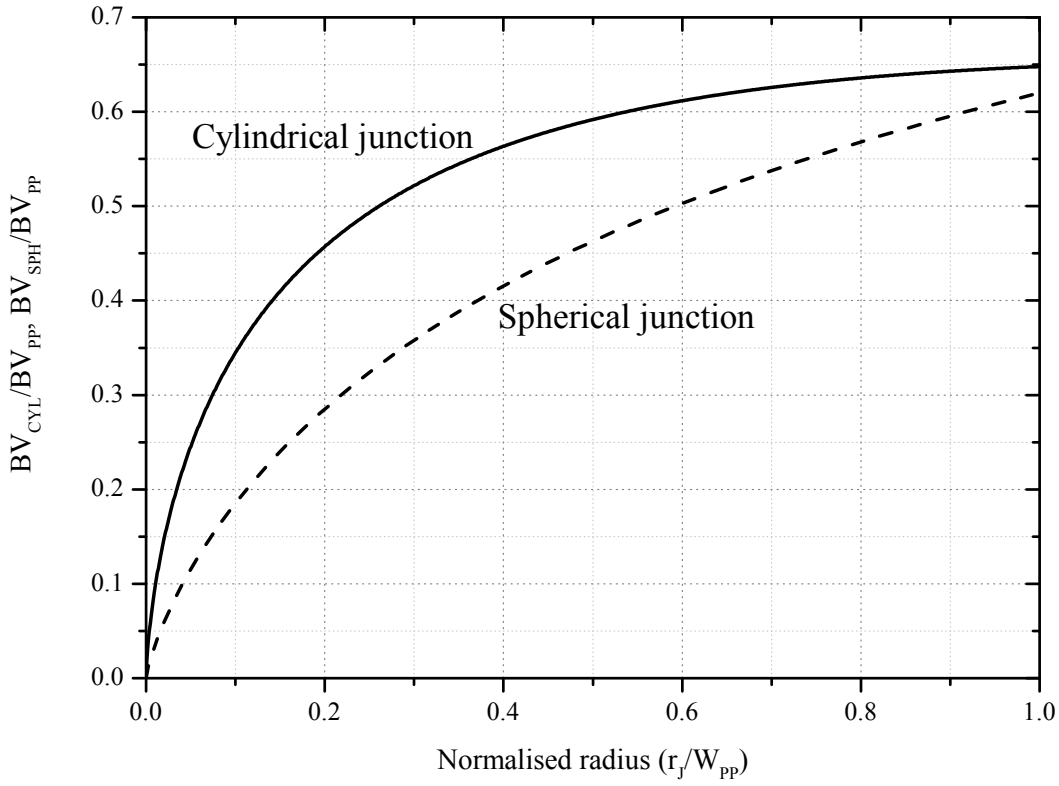


Figure 3.9: Calculated cylindrical and spherical breakdown of a 4H-SiC $P+/N-$ junction.

In order to improve the voltage blocking performance of practical cylindrical junctions,

edge termination designs are required, the purpose of which is to prevent the localisation of electric fields in the device structure by spreading the electric field laterally away from the $P+/N-$ junction. Furthermore, because the breakdown strength of 4H-SiC is similar to that of commonly-used passivation materials (such as SiO_2), the edge termination design that is employed must also ensure that the surface electric field is minimised. In this Section, the principle methods for high voltage edge termination in 4H-SiC devices are discussed and compared.

3.2.1 Floating Field Rings

The floating field ring, illustrated schematically in Figure 3.10, is a simple edge termination method to implement, requiring only a single photolithography and ion implantation process step in an epitaxial anode PiN diode design. As shown in Figure 3.10, the floating field ring structure consists of a series of highly-doped p-type rings that surround the main junction and which are electrically isolated from the anode metal contact, thus allowing the field rings to reach a potential that is intermediate to that of the cathode. Unfortunately, though relatively simple to fabricate, the floating field ring termination has several shortcomings when considering the design of high voltage 4H-SiC devices. Due to the high doping concentration of the implanted field rings, they are not depleted under the application of a reverse bias, and as such do not support significant voltage themselves. The width of the depletion region that actually supports the reverse voltage is found to be [76]

$$W_S' = W_S - \sum W_R \tag{3.57}$$

As such, the design of the floating field ring edge termination requires more die space in order to achieve the same reduction in the surface electric field as other termination

methods in which $W'_S = W_S$.

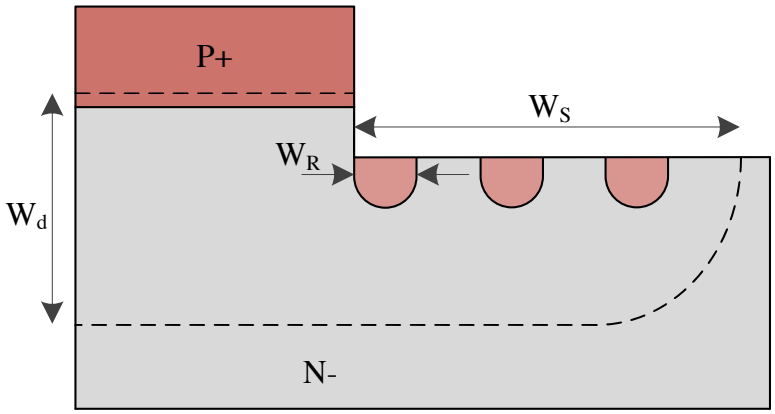


Figure 3.10: Schematic of implanted $P+$ floating field ring termination.

The effectiveness of floating field ring termination in 4H-SiC devices is also hindered by the practical limitation of the implanted junction depth. Since the junction depth is typically limited to below 1 μm in 4H-SiC, precise ring spacing is critical to the performance of the termination structure [77]. Furthermore, because a large number of rings are required for high voltage devices, the design of the termination structure is made difficult due to the fact that the addition of further field rings has an impact on the optimum spacing of all the others. This necessitates complex optimisation of the structure by means of numerical simulations, as discussed in [77]. However, the performance of the floating field ring termination structure is sensitive to the presence of interface charge at the 4H-SiC surface [69]. This charge is highly dependent on device processing conditions, which further complicates the optimisation of this type of termination structure.

3.2.2 Field Plate Termination

Another edge termination technique that has been widely applied in power devices is the field plate, shown schematically in Figure 3.11. When the diode is reverse biased, the voltage on the field plate, which in this case is an extension of the anode contact, is negative with respect to the cathode, which serves to repel electrons away from the surface of the semiconductor and thus expands the depletion region. This results in a reduction of the electric field at the $P+/N-$ junction (point A) and therefore an increase in the breakdown voltage of the device. However, it possible that a high electric field is produced at the edge of the field plate (point B), which can result in premature breakdown at this location.

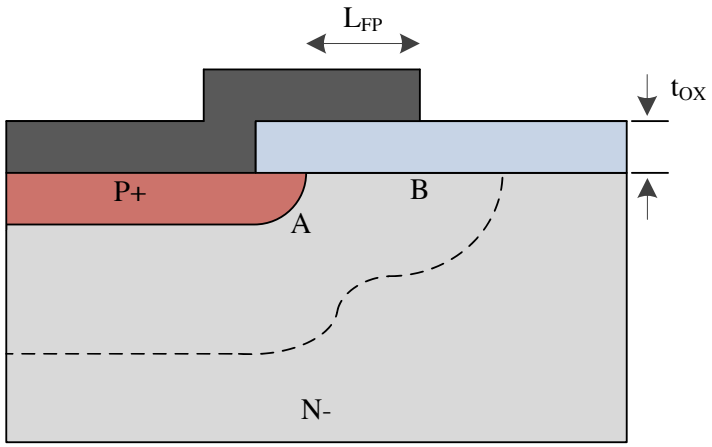


Figure 3.11: Field plate termination for a planar $P+/N-$ junction.

As presented in [69], it can be found that, in accordance with Gauss' law, the electric field within the semiconductor is related to the electric field in the oxide based on the ratio of their respective permittivities. As such, the junction depth that corresponds to

an oxide thickness t_{ox} is given by

$$x_j = \left(\frac{\varepsilon_S}{\varepsilon_{Ox}}\right) t_{ox} \tag{3.58}$$

Based on values of 9.7 and 3.9 for ε_S and ε_{Ox} respectively, it can be seen that the junction depth is approximately 2.5 t_{ox}. As such, for a given oxide thickness, the expected breakdown voltage can be calculated based on the cylindrical junction formulas given in Section 3.2. However, due to the low dielectric constant of SiO_2 compared to that of 4H-SiC, the electric field will be about 2.5 times larger in the SiO_2. Because of this, premature breakdown in the oxide layer is a problem for 4H-SiC power devices with field plate termination. A possible solution to this problem is to use alternative, high-k dielectrics such as aluminium nitride (AlN_x), as presented by Kumta et al. [78].

3.2.3 Bevel Edge Termination

The bevel edge termination is one of the earliest applied methods for terminating high voltage junctions in power devices. Bevelling involves physically modifying the shape of the $P+/N-$ junction in order to minimise electric field at the surface of the semiconductor and prevent field localisation at the edge of the junction. An example of bevel termination is shown diagrammatically in Figure 3.12. This particular example is referred to as a shallow angle negative bevel, as charge is removed from the $P+$ region (with respect to the $N-$ region), and the depletion region can spread laterally. When comparing to the unterminated $P+/N-$ junction example illustrated in Figure 3.8 it can be seen that the surface electric field will be reduced in the bevelled device, as the reverse voltage is now spread over a greater distance.

The major problem with the negative bevel edge termination is that a very shallow

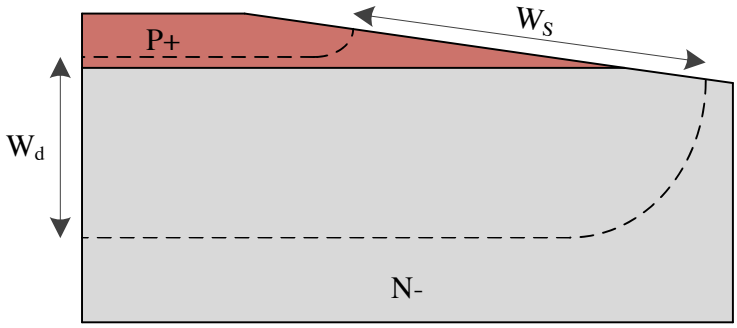


Figure 3.12: Negative bevel edge termination of a $P+/N-$ junction.

bevel angle, of the order 1-5°, is required to sufficiently reduce and spread the electric field away from the main junction [69]. Because of this, negative bevel terminations use a large amount of die area. Furthermore, due to the mechanical and chemical properties of 4H-SiC, bevelling is difficult to implement as, conventionally, processes such as lapping or selective plane wet etching are used to define the shape of the junction. Though these processes are established for Si power devices, they are more challenging for 4H-SiC devices. In addition, the use of bevel edge termination is unsuitable when integrating multiple devices on a single die, which is typically required when prototyping new device designs. As such, bevel terminations typically finds use in high voltage, high current devices, that utilise an entire wafer as a single device.

3.2.4 Junction Termination Extension

The junction termination extension, or JTE, is one of the most commonly used edge termination techniques in SiC power devices. In a JTE, a low-dose implantation is introduced which serves to spread the electric field laterally away from the edge of the main junction. In the case of a $P+/N-$ junction, a p-type implantation is used to provide

ionised acceptors extending away from the main junction, as illustrated in Figure 3.13. The maximum electric field at the junction becomes equal to the critical electric field when the junction reaches its breakdown voltage; under these conditions

$$Q_{OPT} = \varepsilon_S \mathscr{E}_C \approx 1.71 \times 10^{-6} \text{ C/cm}^2 \tag{3.59}$$

where Q_{OPT} is the optimum charge of the implanted JTE region, ε_S is the dielectric constant of 4H-SiC and $\mathscr{E}_C$ is the critical electric field of 4H-SiC, for conservative design purposes assumed to be 2 MV/cm. Based on the calculated value of Q_{OPT}, the required ion implantation dose can be determined

$$Dose = \frac{Q_{OPT}}{q} = 1.07 \times 10^{13} \text{ cm}^{-2} \tag{3.60}$$

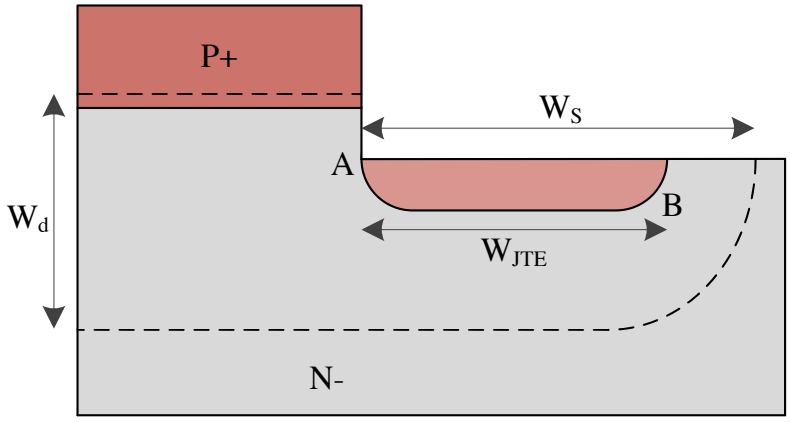


Figure 3.13: Junction termination extension applied to an epitaxial anode PiN diode.

The implanted JTE dose is perhaps the most critical design parameter for achieving high blocking voltages, as if the dose is too low there will be an insufficient amount of N_A^- charge in the depletion region of the JTE, resulting in the electric field localising at the

edge of the main junction leading to breakdown at this point (point A in Figure 3.13). Conversely, if the implanted dose is too high, there will be too much N_A^- charge in the depletion region of the JTE, resulting in breakdown at the far edge of the termination region (point B in Figure 3.13). Another design parameter of the JTE is the width of the JTE window, W_{JTE}; this is designed to be sufficiently wide such that the surface electric field doesn't cause premature failure of the passivation layer. For 4H-SiC devices, it is typical for W_{JTE} to be wide enough such that W_S is several times greater than W_d, and the surface electric field is of the order 1 MV/cm.

As outlined in [79], high voltage devices intending for blocking voltages in excess of 3 kV typically require multiple-zone (MZ) JTE regions, which introduce a decreasing doping concentration laterally away from the main junction or mesa edge, the intention being to gradually spread the electric field away from the main junction, preventing build-up. In order to achieve this, a range of different approaches have been employed. The conventional method is to use a series of masking, etching and implantation steps to create the required charge concentration in each of the JTE zones, as outlined in [76]. However, this method is time-consuming, expensive and introduces uncertainty due to the concentration dependence of the substitutional dopant activation.

In order to overcome the weaknesses associated with the conventional method of obtaining a MZ-JTE, a MZ-JTE design using a single ion implantation stage was developed by Losee [76]. This method used multiple SiO_2 deposition and etch stages to create a SiO_2 layer whose thickness increases laterally in four steps. The SiO_2 layer is then used as the mask for the JTE implantation, with the implanted junction depth in each zone dependent on the thickness of the corresponding SiO_2 mask for that zone. By using a five-stage boron box profile implant, a total implant dose of $7.9\text{x}10^{13}$ cm^{-2} and assuming 25% dopant activation, a blocking voltage of 57% of the parallel plane voltage was achieved.

However, by employing electro-luminescence techniques, it was found that device breakdown under reverse bias typically occurred at the mesa sidewall edge of the JTE, this being attributed to the sharp, high-field corners created by the reactive ion etching (RIE) process used to define mesa areas. In order to mitigate this, highly doped p+ guard rings were incorporated in the first zone of the JTE, thus preventing the JTE from depleting completely to the edge of the RIE mesa etch. These guard ring-assisted MZ-JTE devices were found to safely block over the targeted 10 kV (70% of the parallel-plane voltage). However, the fabrication process required to achieve this JTE structure is still fairly time-consuming due to the multiple SiO_2 deposition, patterning and etching stages required. Furthermore, the controllability of the RIE SiO_2 etch is critical in achieving the correct implant profile depths, thus adding further complexity to the fabrication process.

A different approach to preventing premature breakdown at the device mesa periphery is presented by Hiyoshi et al. [80], who have employed a bevelled mesa structure with a vertical sidewall and gradual slope at the mesa bottom, formed by RIE. This improved mesa structure, in conjunction with a single-zone (SZ) aluminium implanted JTE, allowed the best-performing diodes to achieve a blocking voltage of 10.2 kV, corresponding to approximately 72% of the parallel-plane breakdown voltage and in good agreement with simulations. More recently, in work published by Niwa et al. [81], this bevelled mesa structure has been combined with a dual-implant "space-modulated" JTE to achieve a breakdown voltage of 21.7 kV, which corresponds to 81% of the parallel-plane voltage, and, at the time of writing, is the highest breakdown voltage ever reported for a semiconductor device. This termination method has also been applied to a 4H-SiC BJT device by Miyake et al. [60], again achieving a breakdown voltage in excess of 21 kV.

3.2.5 Surface Passivation

In order to minimise leakage currents and maximise the breakdown voltage of power devices, as well as ensuring their long term reliability, it is necessary to passivate the semiconductor surface. Surface treatment is typically divided into two main steps; the first step is to remove surface contaminants, such as organic particles, metals and oxides, and the second step is to passivate the free dangling bonds of the atoms at the surface of the semiconductor. The aim of the passivation is twofold: to prevent oxidation of the surface in air, and to eliminate electronic surface states. However, though the conventional methodology for Si passivation, whereby hydrogen atoms are attached to Si dangling bonds by dipping in hydrofluoric (HF) acid solution, is established [82], a similar process applied to SiC surfaces has been found to be unsuccessful. One method that has been found to give satisfactory results for SiC surface termination is high temperature (1000°C) annealing in a pure hydrogen atmosphere, though this method comes at the cost of higher processing expense due to the high annealing temperatures that are required.

Once the surface has been terminated, the next stage is to deposit a dielectric layer, which serves to isolate the semiconductor surface from metallisation layers and packaging, as well as passivating the surface to ensure stable and reliable operation of the device. Due to the simplicity of its implementation, SiO_2 has been typically used for the passivation layer of both Si and SiC devices. However, as discussed in Section 3.2.2, the low dielectric constant of SiO_2 compared to SiC implies that the SiO_2 layer is most susceptible to breakdown under high electric fields, again highlighting the need for the use of high-k dielectrics. Another issue with the use of SiO_2 as a dielectric is that sodium (Na) and potassium (K) atoms are known to migrate through the oxide layer, thus creating instability in the breakdown voltage [69]. However, this can be prevented by depositing

a second passivation layer, such as silicon nitride, over the SiO_2.

3.3 Carrier Lifetime in High Voltage 4H-SiC Devices

A major issue that continues to hinder the performance of high voltage 4H-SiC junction rectifiers (as well as other 4H-SiC bipolar devices) is the short carrier lifetime in the drift region of the device. As discussed previously in this Chapter, though these short carrier lifetimes are beneficial for realising low switching losses, too short lifetimes result in excessive on-state losses. In this Section, a mathematical analysis of carrier recombination is first undertaken, in order to quantify the carrier lifetime requirements for the high voltage devices being designed in this work. This is followed by a discussion of the electrically active defects that contribute to the reduction of the carrier lifetime. Finally, methods that have been applied to enhance the carrier lifetime in 4H-SiC are presented.

3.3.1 Carrier Recombination: A Quantitative Analysis

From the PiN diode analysis that has been carried out previously in this Chapter, it can be seen that the performance of these devices is heavily dependent on the carrier lifetime of the material. Regardless of the semiconductor material that is being used for the device, a typical requirement is that the ambipolar (or high-level) lifetime is sufficiently long to yield an ambipolar diffusion length that is comparable to half of the drift region thickness, such that

$$\tau_{HL} = \frac{L_a^2}{D_a} \approx \frac{d^2}{D_a} \tag{3.61}$$

where τ_{HL} is the high-level carrier lifetime, L_a is the ambipolar diffusion length, D_a is the ambipolar diffusion constant and d is half the drift region width. Based on this Equation,

the required high-level carrier lifetime for a range of drift region widths is plotted in Figure 3.14. It can be seen from this Figure that for a 10 kV application, a drift region width of 110 μm would require a high-level lifetime at minimum 5 μs for optimum design tradeoffs. Since the carrier lifetime of as-grown 4H-SiC epitaxial layers is typically less than 1 μs [83], it is evident that some form of post-growth material treatment is necessary if the lifetime is to reach several microseconds. Furthermore, it has been reported that high temperature processing steps, such as those used for implantation activation annealing, can have a severe impact on the carrier lifetime of the material and as such need to be taken into account during the fabrication of high voltage 4H-SiC devices [84].

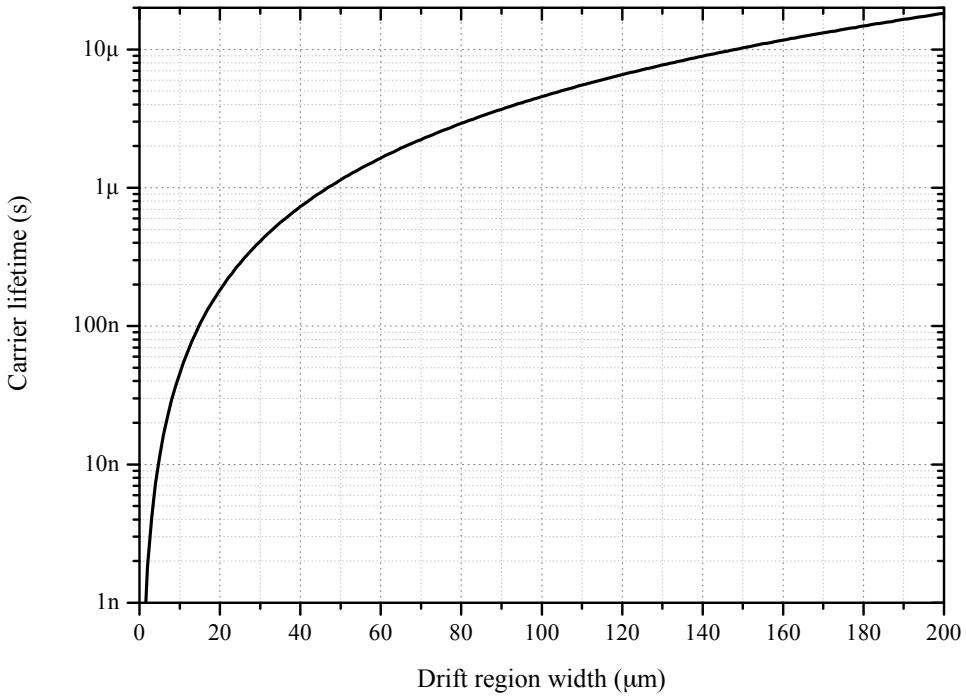


Figure 3.14: Optimum carrier lifetime in 4H-SiC for a range of drift region widths.

By expanding Equation 3.21 to include radiative and surface recombination effects, the overall carrier recombination lifetime in a semiconductor material can be represented

by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{SRH}} + \frac{2S}{W} \tag{3.62}$$

where τ_{Rad} is the radiative recombination lifetime and S is the surface recombination velocity. The first term in the right hand side of Equation 3.62 is the contribution of Auger recombination to the overall lifetime of the semiconductor material. The Auger recombination mechanism is typically dominant in the heavily doped regions of semiconductor devices, or in lightly doped regions under high-level injection conditions, and is represented as outlined in Equation 3.22, repeated here for ease

$$\tau_{Auger} = \frac{1}{\gamma_3 n^2} \tag{3.63}$$

In the work by Galeckas et al. [85] the Auger recombination coefficient γ_3 was calculated to be approximately $7{\times}10^{-31}$ cm^6/s; this was based on measurements taken using a time-resolved photo-induced absorption technique. As demonstrated in [85], the Auger recombination in 4H-SiC is negligible for carrier densities less than 10^{18} cm^{-3}.

The second term in Equation 4.13 represents the radiative recombination component, which is typically considered to be negligible in indirect band gap semiconductor materials, such as Si and 4H-SiC. As with Auger recombination, the radiative recombination component of the overall carrier lifetime in 4H-SiC has been found to be negligible for carrier concentrations less than 10^{18} cm^{-3}. The next term is the lifetime component due to SRH recombination, arising due to defect levels present in the material. Because it is this recombination component that usually dominates the lifetime in the drift region under normal operating conditions, it is particularly crucial to the electrical performance of high voltage PiN diodes. The SRH lifetime parameters are expressed mathematically

as [42]

$$\tau_{n0} = \frac{1}{\sigma_{n0} N_t \nu_{n,th}} \tag{3.64}$$

for electrons, and

$$\tau_{p0} = \frac{1}{\sigma_{p0} N_t \nu_{p,th}} \tag{3.65}$$

for holes, where N_t is the defect concentration, σ is the defect capture cross section and ν_{th} is the carrier thermal velocity. When the PiN diode is operated under high-level injection conditions, the high-level lifetime in the drift region of the device can be represented by

$$\tau_{HL} = \tau_{n0} + \tau_{p0} \tag{3.66}$$

As such, in order to achieve longer carrier lifetimes, the defect concentration N_t needs to be reduced. As reported by Kumar et al. [86], based on the capture cross section of known defects in 4H-SiC, the defect concentration in the material should be less than $\approx 10^{12}$ cm^{-3} if SRH recombination-limited high-level lifetimes in the microsecond range are to be achieved. These defects are discussed in the next Section.

3.3.2 The Effect of Electrically Active Defects on Carrier Lifetime

The various defects and impurities observed in 4H-SiC have been widely studied, and are discussed in numerous publications [71, 87–89]. Other than the intentionally-introduced shallow impurities that define the conductivity type of the semiconductor, both intrinsic and extrinsic deep defect levels have been found in doped and undoped 4H-SiC. Extrinsic deep defect levels are defined as impurities which are introduced (either intentionally or unintentionally) during the doping process of the semiconductor; such defect levels are

unintentionally incorporated during bulk or epitaxial material growth due to residual contamination of the growth reactor. Three of the most common residual impurities in 4H-SiC crystals are the transition metals titanium (Ti), vanadium (V) and chromium (Cr), the electrical properties of which are outlined in Table 3.1. It was suggested in [90] that the deep level due to the presence of vanadium in SiC is an efficient recombination centre, thus limiting the lifetime of the material or compensating shallow donors. Because of this, vanadium has been successfully applied in the production of semi-insulating SiC substrates.

Table 3.1: Summary of the electrical properties of extrinsic defects observed in 4H-SiC. The indices (h) and (c) indicate the electrical properties for impurities residing on hexagonal and cubic lattice sites respectively.

Defect	Location in band gap (eV)	Capture cross section (cm^2)	Ref.
Titanium (h)	$E_C - (0.11\text{-}0.13)$	$2\times10^{-15} - 1\times10^{-14}$ (electron)	[89]
Titanium (c)	$E_C - (0.15\text{-}0.17)$	$3\times10^{-15} - 2\times10^{-14}$ (electron)	[89]
V	$E_C - 0.97$	6×10^{-15}(electron)	[87]
Cr	$E_C - (0.15\text{-}0.74)$	$8\times10^{-16} - 2\times10^{-15}$ (electron)	[87]

Intrinsic defects (also referred to as point defects) in a semiconductor are defined as imperfections in the crystal, in the form of vacancies, anti-sites, and interstitials. Vacancies are, as their name suggests, atomic sites on which no atom is present; conversely, interstitials are formed by the introduction of an atom into a non-lattice site within the crystal. Anti-site defects are formed through atoms residing on the wrong sub-lattice site; in SiC this could be either a carbon anti-site (where a carbon atom resides on a silicon site) or a silicon anti-site (where a silicon atom resides on a carbon site). Intrinsic defects have been studied intensely in both as-grown and epitaxial SiC material, as well as in material subjected to ion implantation and electron or proton irradiation processes. A summary of the electrical properties of these intrinsic defects is given in Table 3.2.

Table 3.2: Summary of electrical properties of intrinsic defects observed in 4H-SiC.

Defect	Location in band gap (eV)	Capture cross section (cm^2)	Ref.
$Z_{1/2}$	$E_C - (0.63\text{-}0.68)$	$3\times10^{-15} - 2\times10^{-14}$ (electron)	[89]
EH_6	$E_C - 1.203$	1.2×10^{-16} - 4.7×10^{-16} (electron)	[91]
EH_7	$E_C - 1.58$	1.9×10^{-14} - 7.1×10^{-16} (electron)	[91]
Shallow boron	$E_V + (0.23\text{-}0.28)$	$2\times10^{-14} - 3\times10^{-13}$ (hole)	[89]
HS1	$E_V + 0.35$	2×10^{-14} (hole)	[89]
D center	$E_V + 0.49$	1×10^{-16} (hole)	[92]
P1	$E_V + 1.49$	8×10^{-15} (hole)	[93]

Of these intrinsic defects that have been observed in 4H-SiC, the dominant lifetime-killing defect is the $Z_{1/2}$ defect, which is considered to be a carbon vacancy-related defect [83]. In addition, the EH_6 defect, which is also suspected to be a carbon vacancy-related defect alongside another component available at high concentration, such as nitrogen or a second carbon vacancy [91], has also been found to have an inverse correlation with the carrier lifetime in the semiconductor. As such, it is crucial that the concentration of these two defects is reduced in the semiconductor if high carrier lifetimes are to be obtained. Methods to achieve this lower defect concentration in 4H-SiC, and thus enhance the carrier lifetime of the material, are discussed in the following Section.

3.3.3 Carrier Lifetime Enhancement

In order to reduce the concentration of the aforementioned lifetime-killing defects in 4H-SiC, and thus increase the carrier lifetime in the material, some post-growth processing needs to be applied. As outlined in the previous Section, the dominant lifetime-killing defects in 4H-SiC, the $Z_{1/2}$ defect and the $EH_{6/7}$ defect, are both reported to be carbon vacancy-related. As such, methods to 'repair' the $Z_{1/2}$ and $EH_{6/7}$ defects involve the diffusion of carbon interstitials from near the surface of the semiconductor into the bulk of the material. These carbon interstitials are generated by means of either carbon

implantation [94], or thermal oxidation [4].

In the carbon implantation method reported in [94], a 250 nm carbon box profile was implanted into the 4H-SiC epilayer, creating a region with an excess of carbon interstitials. A range of annealing temperatures were investigated (between 800°C and 1800°C) for the diffusion of the excess carbon interstitials into the semiconductor bulk, and samples were characterised using deep level transient spectroscopy (DLTS) and time resolved photoluminescence (TRPL) to determine the defect concentration in the semiconductor. It was found that for annealing temperatures of 1600°C and above, the DLTS spectra peaks dropped below the detection limit for both the $Z_{1/2}$ and $EH_{6/7}$ defects, and the carrier lifetime of the material doubled in the implanted and annealed samples when compared against unimplanted reference samples. This carbon implantation and annealing technique was applied to thick ($\sim$265 μm) epitaxial layers in [95]; in this work the carrier lifetime was increased from $\sim$3.5 μs in the as-grown samples to $\sim$18.5 μs in the implanted samples.

In the work by Hiyoshi and Kimoto [4], the use of thermal oxidation was applied to reduce the concentration of the $Z_{1/2}$ and $EH_{6/7}$ defects in 4H-SiC epitaxial layers and thus improve the carrier lifetime. The thermal oxidation process results in carbon interstitials being generated at the SiO_2/SiC interface, which diffuse into the bulk and occupy carbon vacancy sites related to $Z_{1/2}$ and $EH_{6/7}$ defect centres during the process. By performing two 5 hour 1300°C thermal oxidations (removing the grown SiO_2 between the two stages), the carrier lifetime of the material was increased from 0.73 μs in the as-grown material to 1.62 μs after oxidation, with the $Z_{1/2}$ defect centre found to be below the detection limit to a depth of 50 μm in the semiconductor.

Though the thermal oxidation process described in [4] was successful in reducing the $Z_{1/2}$ and $EH_{6/7}$ concentrations, it was found that another defect centre, HK0, is generated

during the process [96], estimated from the DLTS spectra to be at an energy level of $E_V + 0.78$ eV. Interestingly, the HK0 concentration was highest near the the oxidised surface of the semiconductor, gradually decreasing with increasing depth into the material bulk, whilst the $Z_{1/2}$ concentration displayed the opposite trend, increasing to the value of the as-grown epitaxial layer at the depth where the HK0 concentration decreased to the detection limit (6-7 μm), thus suggesting interaction between the $Z_{1/2}$ and HK0 centres during the thermal oxidation process. It was reported in [92] that the HK0 defect centre could be annealed out in an inert ambient at 1550°C; this was applied after the thermal oxidation process in [96] and the carrier lifetime was found to increase from 2.54 μs after the thermal oxidation to 4.52 μs. This was a seven-fold increase when compared to the lifetime of the as-grown sample.

3.4 4H-SiC Device Fabrication Technology

3.4.1 Etching of 4H-SiC

Due to its chemical inertness, it is difficult to etch 4H-SiC in conventional acid or base solutions, like can be done for Si. Wet etching of SiC requires the use of molten salts, such as potassium hydroxide (KOH) or sodium hydroxide (NaOH), at high temperatures, typically 600-800°C. As such, it is favourable to employ dry, plasma-based etching techniques. Similar to Si dry etching, typical SiC dry etch chemistries are based on fluorinated plasmas such as tetrafluoromethane (CF_4), though the optimisation of etch processes differs slightly due to the fact that the SiC is a source of C, meaning different C:F ratios are required.

The earliest and most commonly reported dry etching method applied to SiC was reactive ion etching (RIE) [97, 98]. However, due to the nature of the RIE process, whereby ions physically bombard the SiC surface to etch it away, the resulting surface damage is relatively high, and recombination centres are generated. Due to this increased surface recombination, the overall carrier lifetime in the device is decreased. As such, the use of high-density plasma source etching methods, such as inductively coupled plasma (ICP) etching, has been favoured over RIE, and excellent results, in terms of etch rates and surface roughness, have been reported [99]. In [99], a CF_4/O_2-based ICP etch was investigated and optimised; this has since been demonstrated in the fabrication of a range of high voltage 4H-SiC power devices [100,101]. As such, for the devices fabricated in this research, ICP etching of 4H-SiC has been employed.

3.4.2 Ion Implantation and Activation Annealing

Unlike for Si semiconductor technology, where thermal dopant diffusion is a well-established and effective process for realising selectively doped regions in a device, this dopant diffusion process cannot be simply applied to the fabrication of 4H-SiC devices. This is due to the low diffusion coefficients of the main dopant species that are needed for the fabrication of 4H-SiC semiconductor devices, meaning that temperatures in excess of 2000°C would be required. As such, ion implantation is the most widely applied technology used for realising doped regions in 4H-SiC devices.

Achieving these doped regions in 4H-SiC devices is further complicated by the fact that the implanted dopant species have a limited projected range when compared to dopants in Si. This necessitates the use of higher implant energies, in the range of keV-MeV, to achieve sufficiently deep junctions for power devices. However, these junction depths are

typically limited to below 1 μm, which, as discussed in Section 3.2, can degrade the two-dimensional blocking capability of the device by enhancing electric field crowding at the junction periphery. The common p-type dopants for 4H-SiC devices are aluminium (Al) and boron (B), though with its lower atomic mass boron is the preferred option for forming deeper junctions. Based on SRIM [102] simulations, boron has a projected range of $\sim$0.6 μm at an implant energy of 360 keV, compared to $\sim$0.4 μm for aluminium. However, though boron has this junction depth advantage over aluminium, aluminium has the advantage of having a shallower ionisation energy with respect to the edge of the valence band in 4H-SiC ($\sim$220 meV for aluminium compared to $\sim$330 meV for boron [103]), meaning that larger p-type carrier concentrations in the freeze-out temperature region are realised. As such, lower sheet resistances are achievable with aluminium-doped 4H-SiC when compared to boron-doped 4H-SiC.

For the doping of n-type 4H-SiC, nitrogen and phosphorous are the most commonly used implanted species. At an implant energy of 360 keV, these dopant species have projected ranges of $\sim$0.5 μm and $\sim$0.3 μm respectively, making nitrogen more suitable when deep junctions are required. In terms of their ionisation energies, it is found that they are both significantly lower than for p-type dopants, being under 100 meV [104]. However, as reported in [105], phosphorous implants achieve sheet resistance values approximately an order of magnitude lower than that which is achieved for nitrogen implants. This is due to the higher activation ratio of implanted phosphorous compared to nitrogen, which is explained by the fact that at high doses the formation of N_2 molecules or other nitrogen-containing particles reduces the concentration of nitrogen that is available to become electrically active.

One of the principle advantages of ion implantation is that it allows accurate control of the charge introduced into the semiconductor material. However, the implantation process

causes damage to the crystal structure of the semiconductor, with C and Si atoms being knocked out of their lattice positions and ending up on interstitial lattice sites. The magnitude of this damage is dependent on the dopant ion species mass, the implantation energy and the implanted dose. It has been found that implantation at higher energies causes greater damage to both the semiconductor surface and lattice, and also creates defects in the implanted regions of the semiconductor material [106], having implications for the overall carrier lifetime in the material, and hence device performance.

It is found that only a minority of implanted dopant atoms will end up on substitutional lattice sites where they are electrically active, with the majority of dopant atoms occupying interstitial lattice sites and thus being electrically inactive [107]. To activate these dopant atoms as well as reducing the damage in the semiconductor crystal, a high temperature thermal annealing step is required. For activation of n-type dopants an anneal temperature of $\sim$1300°C is required; for p-type dopant activation the anneal temperatures are significantly higher, being found to be $\sim$1500°C and $\sim$1700°C for aluminium and boron respectively [108]. However, when performed without any protection of the semiconductor surface, these high temperature anneals have been found to cause "step bunching", which is a roughening of the SiC surface due to the sublimation and redeposition of Si. Furthermore, out-diffusion of dopants is also a problem during high temperature annealing. In order to prevent this, some form of capping layer is used; layers such as aluminium nitride (AlN) [109] and graphite (converted from photoresist) [110] have both been applied and found to prevent both the step bunching effect and, in most cases, dopant out-diffusion during high temperature annealing, though AlN was unsuccessful in preventing boron out-diffusing.

Another implication of the high temperature activation anneal required for p-type dopant activation, and one which is particularly important for high voltage bipolar power

devices, is that annealing temperatures in excess of 1600°C have been found to increase the concentration of the $Z_{1/2}$ and $EH_{6/7}$ defects in the semiconductor, and thus have a negative impact on the carrier lifetime of the material [84]. Assuming that the implant activation anneal cannot be performed prior to the carrier lifetime enhancement process, a lower temperature anneal should be performed with the trade off of a reduced concentration of activated dopants. However, the use of high temperature ion implantations can assist in promoting the implanted dopant species to reside in active lattice sites [111].

3.4.3 Ohmic Contacts to 4H-SiC

It is well documented that the formation of reliable, low resistance ohmic contacts to 4H-SiC, particularly p-type 4H-SiC, is difficult. Low contact resistances are necessary if low on-state power losses are to be minimised, and are also required if high switching speeds are to be realised. The typical process that is applied to form ohmic contacts on 4H-SiC is to deposit suitable metals over heavily doped n- or p-type device regions, then perform a post-deposition anneal. Though it is found that most 'as-deposited' metals form rectifying (Schottky) contacts to 4H-SiC, a short high temperature anneal typically allows ohmic contacts to be achieved. The contact resistance is dependent on several factors; these include the contact metal (or metals) used, the doping concentration of the semiconductor, surface treatment prior to metal deposition, and the annealing conditions used.

The formation of ohmic contacts to n-type SiC is a subject that has been widely studied in recent years [112–114]. Though early work primarily focused on ohmic contacts to 6H-SiC [115], the improvements in 4H-SiC substrate and epitaxy quality since then meant that the focus shifted to this material. Much of the work on n-type ohmic contacts has

involved the use of nickel (Ni) and Ni-based alloys for the contact metal, though a range of other metals, such as titanium (Ti), tantalum (Ta), niobium (Nb) and molybdenum (Mo), have also been successfully employed [116]. The review of ohmic contacts to n-type 4H-SiC in [116] illustrates that specific contact resistances of the order 10^{-6} $\Omega{\cdot}\text{cm}^2$ are typical, with the lowest figure reported being $2.7{\times}10^{-7}$ $\Omega{\cdot}\text{cm}^2$.

Though there have been reports of work in which ohmic contacts to n-type 4H-SiC have been achieved without any post-deposition annealing processes [116], the vast majority of reported work has involved an anneal process of some description. The anneal parameters, such as temperature, duration and annealing atmosphere, are dependent on the types of metal used for the contact, though anneals are typically carried out between 900-1100°C for 1-10 minutes in either an argon (Ar) atmosphere or under vacuum, to prevent oxidation of the metal surface at these elevated temperatures. In the case of the Ni contact, the high temperature anneal process results in the formation of silicides (Ni_2Si), which have been found to lower the Schottky barrier height and thus reduce the contact resistance [116]. However, due to poor morphology and long-term stability of Ni-only ohmic contacts [113, 117], it is preferable to use a multilayer metallisation scheme, such as Ti/Ni/Al, Al/Ni/Al and Ni/Ti, in order to improve the morphology and long-term stability of the contact.

As mentioned previously, low resistance ohmic contacts to p-type 4H-SiC are harder to achieve than for n-type material. The main reason for this is because of the wide band gap of 4H-SiC, which results in a large Schottky barrier height at the metal-semiconductor interface. This potential barrier is unavoidable, since the valence band edge for 4H-SiC is located approximately 7 eV below the vacuum level, and the maximum work function of any known metal is less than 6 eV [118]. As such, in order to promote ohmic behaviour, the semiconductor underneath the contact is heavily doped so as to facilitate field emission

current transport through the potential barrier [119]. However, due to the poor dopant ionisation of acceptors at room temperature, heavily doped p-type regions in 4H-SiC are difficult to obtain in practice.

Because Al is a p-type dopant, it was thought that its use as an anode contact metal would promote low resistance ohmic contacts by doping the 4H-SiC during a high temperature annealing process and thus facilitating field emission through the metal-semiconductor interface [118]. Though this has since been discounted, Al is still widely used in ohmic contacts to p-type 4H-SiC due to its ability to promote the formation of Schottky barrier-lowering compounds at the metal-semiconductor interface [120]. As discussed in [121], metallisation schemes based on Ti/Al alloys have yielded the best results in terms of specific contact resistance, both for epitaxial and implanted p-type 4H-SiC layers. This correlates with the results obtained by Jennings et al. [3], who found that a Al/Ti/Al metallisation scheme yielded the lowest specific contact resistance, at 5.0×10^{-6} $\Omega\cdot\text{cm}^2$. However, it is evident from the literature that even for similar metallisation schemes and annealing conditions, the resistance values that are reported by different research groups vary significantly (around two orders of magnitude), suggesting that the semiconductor material quality and the pre-deposition surface treatment process both play an important role in achieving low resistance ohmic contacts.

3.5 A Review of High Voltage 4H-SiC PiN Diode Technology

Although in recent years there has been significant global research activity in the field of 4H-SiC PiN diodes, no commercial devices are on the horizon as yet. This can be primarily

attributed to the presence of stacking faults originating from BPDs in the semiconductor material, which, as discussed in Chapter 2, result in the deterioration of forward I-V characteristics over time. Though the quality of 4H-SiC substrates has improved greatly over the past few years, this is still an issue that hinders the performance of bipolar devices, particularly high voltage devices with thick epitaxial layers. A recent study of the influence of stacking faults on the electrical performance of high voltage 4H-SiC PiN diodes was undertaken by Nakayama et al. [122], who investigated the effect that 8H-type in-grown stacking faults (IGSFs) had on the forward characteristics of epitaxial PiN diodes with carbon-implantation for carrier lifetime enhancement. Using the carbon implantation process outlined in [94], a carrier lifetime in excess of 10 μs is expected, meaning that the forward voltage drop of the diode at 100 A/cm^2 should be around 3 V at 25°C. This process was applied to two samples, one with no IGSFs, and one with an IGSF density of >500 cm^{-1}. Whilst the sample with no IGSFs had a forward voltage drop of around 2.7 V at 100 A/cm^2 and 250°C, the sample with a high IGSF density exhibited significantly worse characteristics, with a voltage drop of around 30 V at just 35 A/cm^2 (and 250°C). This illustrates the detrimental effect that IGSF density has on the carrier lifetime of the device, and the importance of decreasing IGSFs in high voltage 4H-SiC PiN diodes.

Because these lifetime-killing stacking faults originate from BPDs, a potential solution is to use low off-cut angle substrates. In [123], 13 kV 4H-SiC PiN diodes have been fabricated on both 4° and 8° off-axis substrates, and their electrical properties compared. All of the fabricated devices exhibited similar reverse characteristics regardless of the substrate off-axis angle, though the devices fabricated on 8° off-axis substrate were found to have slightly better initial forward characteristics, with a differential on-resistance $R_{on,diff}$ of 14.3 mΩ-cm^2 compared to 17.0 mΩ-cm^2 for the devices fabricated on the 4°

off-axis substrate. However, after application of DC bias stress, the devices from the 8° off-axis substrate exhibited more severe forward voltage degradation than those from the 4° off-axis substrate. As such, lower off-axis angle substrates are preferable for minimising the detrimental effect of stacking faults on device performance, which correlates with the results presented in [124]. Following a similar idea, Civrac et al. fabricated 4H-SiC PiN diodes on on-axis substrates [125]. However, when compared to off-axis epitaxial layers, the on-axis epitaxial layers were found to be relatively inhomogeneous and rough, which is attributed to the defects present and the surface roughness of the on-axis substrate prior to epitaxial growth [126]. Electrical characterisation of these devices found both the forward and reverse characteristics of the devices fabricated on the on-axis substrate were inferior to the devices fabricated on the off-axis substrate.

Researchers at Cree, Inc., in conjunction with the Army Research Laboratory (USA), have recently published their latest efforts in 4H-SiC PiN diode technology, in the form of a 16 kV device with an active area of 0.5175 cm^2 [127]. These devices underwent a carrier lifetime enhancement process during the fabrication process, and exhibited a $R_{on,diff}$ of around 9.5 mΩ-cm^2 at 100 A/cm^2 and 25°C, dropping to around 7 mΩ-cm^2 at 200°C. The improved forward I-V performance of the diodes indicates that the high-level carrier lifetime in the semiconductor improves with increasing temperature; however, for a given temperature, it was also observed that $R_{on,diff}$ dropped with increasing current density, suggesting that the carrier lifetime needs to be further increased in order to improve the conductivity modulation at lower current densities. Regarding the reverse blocking characteristics of the fabricated PiN diodes, the use of a negative bevel mesa termination allowed the devices to block 16 kV with a reverse leakage current of just 0.9 μA.

In [128], Snook et al. presented a 1.8 kV / 64 kA 4H-SiC PiN diode based on multiple interconnected devices on a 3-inch wafer, forming a 11.72 cm^2 wafer-scale diode. The

size of each individual diode was optimised based on defect distribution calculations, with an active area of 0.09 cm^2 (0.17 cm^2 total area including edge termination) being found to be the optimum size for maximising area and yield. After the anode metallisation process, a breakdown voltage test was performed on each diode, in order to select devices for interconnection. Based on a leakage current density of 0.2 mA/cm^2 at the breakdown voltage of 1.8 kV, a yield of 83% was achieved. The individual diodes that passed the criteria were then interconnected to form the large area device, with the excluded devices remaining inactive. This PiN diode was found to have a forward voltage drop of 10.3 V at a pulsed peak current of 64.3 kA, corresponding to a peak current density of around 5.5 kA/cm^2 and a $R_{on,diff}$ of around 1.9 $m\Omega$-cm^2 (assumedly at room temperature, though this is not specified).

In terms of breakdown voltage, the highest-rated devices to date have been fabricated by researchers at Kyoto University, Japan, who have reported a PiN diode with a breakdown voltage of 21.7 kV [81]. Both experimental and simulation data showed that the breakdown voltage of PiN diodes with a conventional single-zone JTE (SZ-JTE) was heavily sensitive to not only the JTE dose, but also the charge at the SiO_2/SiC interface. Using the SZ-JTE, a breakdown voltage of around 12 kV was achieved at an implant dose of 1.2×10^{13} cm^{-2}, though this dropped to around 8 kV at a reduced dose of 1.0×10^{13} cm^{-2}, and dropped further to around 4 kV with a increased dose of 1.4×10^{13} cm^{-2}.

To reduce the sensitivity to the JTE dose and interface charge, both a two-zone JTE (TZ-JTE) and a space-modulated two-zone JTE (SM-TZ-JTE) were incorporated into fabricated devices. The SM-TZ-JTE is shown schematically in Figure 3.15, and utilises two overlapping implants to obtain a JTE dose that decreases away from the $P+/N-$ junction. Using this termination structure the sensitivity was decreased significantly and the achievable breakdown voltage was hugely increased; simulation results showed

that at a dose of 1.2×10^{13} cm^{-2} a breakdown voltage of around 26 kV was achieved, dropping to just 25 kV at 1.0×10^{13} cm^{-2} and to 22 kV at 1.4×10^{13} cm^{-2}. When evaluated experimentally, the PiN diodes with the SM-TZ-JTE structure were found to block a reverse voltage of 21.7 kV with a reverse leakage current of less than 200 μA/cm^2.

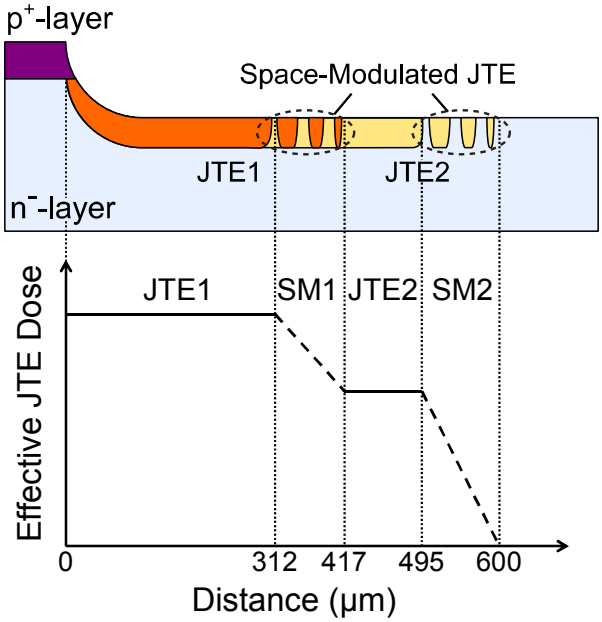


Figure 3.15: Schematic of cross-section of SM-TZ-JTE structure (taken from [81]).

3.6 Summary

In this Chapter, the technical aspects of high voltage 4H-SiC PiN diodes have been presented. This has involved a detailed analysis of the forward, reverse blocking and reverse recovery behaviour of PiN diodes, which will be applied when evaluating the characteristics of fabricated devices. Design aspects that are crucial to the performance of high voltage 4H-SiC power semiconductor devices, namely edge termination and carrier lifetime enhancement were discussed next, with the most promising options being identified

for incorporation into the devices to be fabricated. Similarly, aspects of semiconductor device processing that are necessary for the PiN diodes being fabricated were discussed, and again the most suitable options were highlighted. Finally, a review of the current state-of-the-art of high voltage 4H-SiC PiN diodes has been presented, illustrating recent achievements in the field, in addition to technical issues that are yet to be resolved.

Chapter

4 Design and Simulation of High Voltage 4H-SiC PiN Diodes

In this Chapter, the design and optimisation of high voltage 4H-SiC PiN diodes is presented. First, the analytical models that are used in numerical (ATLAS) simulations are outlined. Following this, the first stage in device design, which involves determining the optimum drift region specification needed to support the target reverse blocking voltages, is presented. Once the drift region designs have been determined, numerical simulations are next undertaken, the aim of which is twofold. Forward I-V simulations are performed, in order to ascertain the carrier lifetime required in the devices to obtain the optimum on-state performance of the PiN diodes. After the forward I-V simulations, reverse breakdown simulations are carried out for both 3.3 kV and 10 kV-rated PiN diodes, investigating the performance of various JTE structures in terms of the maximum achievable reverse breakdown voltage for the devices.

4.1 Numerical Simulation Models

In order to design semiconductor devices using numerical simulations, a reliable set of material parameters and physical models are required. In this Section, the important 4H-SiC material parameters and models used in the ATLAS [129] simulations in this work are outlined.

4.1.1 Band Gap Narrowing

In the simulation of semiconductor devices, the most fundamental property of a material is its band structure. The band gap of a semiconductor is inherently dependent on both impurity concentration and temperature [130], and, as such, it is crucial that this is accounted for in numerical simulations. This is of particular importance for 4H-SiC, where some of the material advantages, such as its wide band gap and low intrinsic carrier concentration, could be diminished at high temperatures or in heavily doped regions of the device. The band structure for 4H-SiC is illustrated in Figure 4.1 [131]. The temperature dependence of the band gap energy is modelled in ATLAS as shown in Equation 4.1, and the parameters for 4H-SiC, based on those given in [103], are outlined in Table 4.1. This temperature dependence of the band gap energy (E_G) of 4H-SiC is illustrated in Figure 4.2.

$$E_G(T_L) = E_G(300) + \alpha \left[\frac{300^2}{300 + \beta} - \frac{T_L^2}{T_L + \beta} \right] \tag{4.1}$$

As outlined above, experimental work has shown that as the dopant impurity concentration in a semiconductor material increases, the band gap separation energy decreases, whereby the conduction band is lowered by approximately the same amount as the valence band is raised. A model for the doping-induced band gap narrowing in 3C-, 4H-

Table 4.1: Band gap narrowing temperature dependence parameters.

Parameter	Units	Value
$E_G(300)$	eV	3.26
α	eV/K	3.3×10^{-2}
β	K	1.0×10^{5}
T_L	K	4-700

and 6H-SiC, along with the fitting parameters, is given by Lindefelt [130]. According to this model, the downward shift of the conduction band in n-type material is given by

$$\Delta E_{Cn} = BGN.LIND.ANC \left(\frac{N_D^+}{BGN.LIND.ND} \right)^{1/3} + BGN.LIND.BNC \left(\frac{N_D^+}{BGN.LIND.ND} \right)^{1/2} \tag{4.2}$$

and the upward shift of the valence band in n-type material is given by

$$\Delta E_{Vn} = BGN.LIND.ANV \left(\frac{N_D^+}{BGN.LIND.ND} \right)^{1/4} + BGN.LIND.BNV \left(\frac{N_D^+}{BGN.LIND.ND} \right)^{1/2} \tag{4.3}$$

where N_D^+ is the ionised donor concentration. Correspondingly, for p-type material, the downward shift in the conduction band is given by

$$\Delta E_{Cp} = BGN.LIND.APC \left(\frac{N_A^-}{BGN.LIND.NA} \right)^{1/4} + BGN.LIND.BPC \left(\frac{N_A^-}{BGN.LIND.NA} \right)^{1/2} \tag{4.4}$$

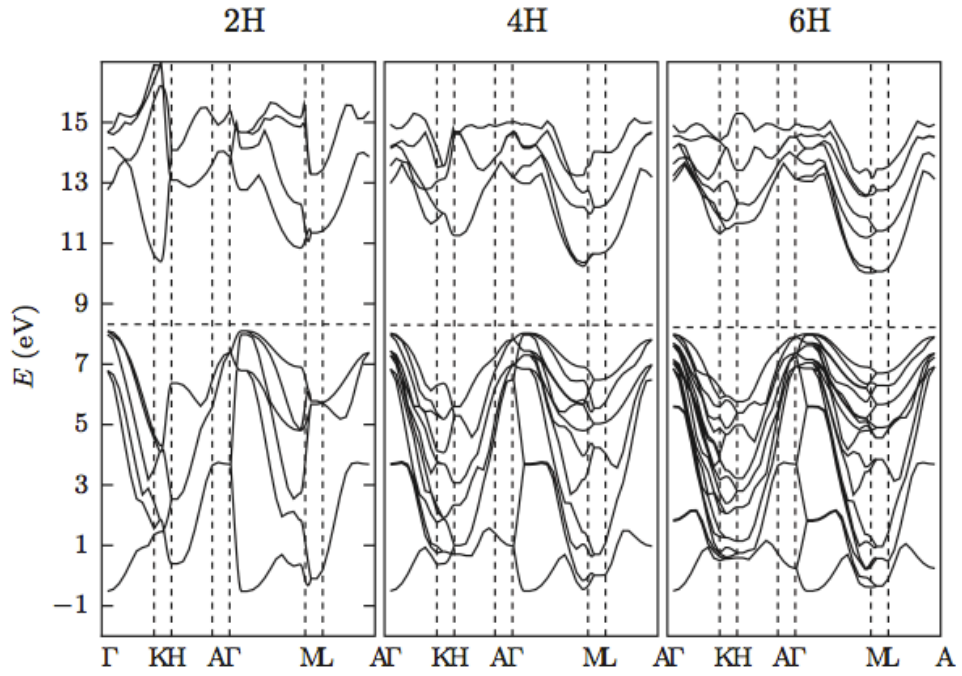


Figure 4.1: Electronic band structure for 2H, 4H- and 6H-SiC calculated using density functional theory (DFT) [131].

and the upward shift in the valence band in p-type material is given by

$$\Delta E_{Vp} = BGN.LIND.APV \left(\frac{N_A^-}{BGN.LIND.NA} \right)^{1/2} + BGN.LIND.BPV \left(\frac{N_A^-}{BGN.LIND.NA} \right)^{1/2} \tag{4.5}$$

where N_A^- is the ionised acceptor concentration. The band gap energy is therefore given by

$$\Delta E_{G,n-type} = E_G - |\Delta E_{Cn} + \Delta E_{Vn}| \tag{4.6}$$

for n-type material, and

$$\Delta E_{G,p-type} = E_G - |\Delta E_{Cp} + \Delta E_{Vp}| \tag{4.7}$$

for p-type material. The parameters for 4H-SiC for the band gap narrowing doping dependence model are given in Table 4.2, and the effects of doping concentration on the band gap energy of 4H-SIC as described by the above model are illustrated in Figure 4.3.

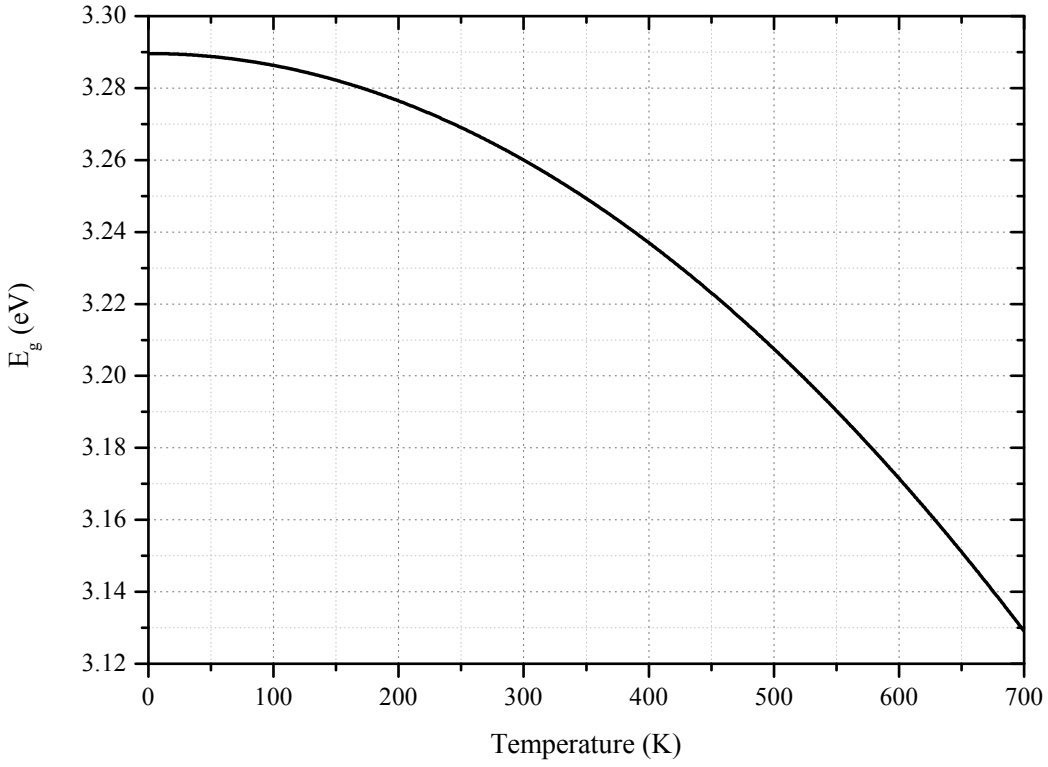


Figure 4.2: Effect of temperature on the band gap energy of 4H-SiC.

Table 4.2: Band gap narrowing doping dependence parameters [130].

Parameter	Units	Value
$BGN.LIND.ANC$	eV	1.50×10^{-2}
$BGN.LIND.BNC$	eV	2.93×10^{-3}
$BGN.LIND.ANV$	eV	1.90×10^{-2}
$BGN.LIND.BNV$	eV	8.74×10^{-3}
$BGN.LIND.APC$	eV	1.57×10^{-2}
$BGN.LIND.BPC$	eV	3.87×10^{-4}
$BGN.LIND.APV$	eV	1.30×10^{-2}
$BGN.LIND.BPV$	eV	1.15×10^{-3}

4.1.2 Carrier Transport

In a semiconductor material the carrier mobility is dependent on a number of factors, including lattice temperature, electric field and dopant concentration due to various scattering mechanisms such as phonons, impurity ions, surfaces, and other material imperfections. At low electric fields, the drift velocity v_d is proportional to the electric field strength $\mathscr{E}$, with the proportionality constant defined as the mobility μ, or

$$v_d = \mu\mathscr{E} \tag{4.8}$$

The value of this mobility has a characteristic low-field value that is denoted by the symbol μ_n, μ_p, for n-type and p-type material respectively. This low-field mobility value is dependent upon phonon and impurity scattering, which both act to decrease the low-field mobility. A widely-used approach to model this dependence is given by the Caughey-Thomas mobility model [132]

$$\mu_0 = \mu_{min} + \left[\frac{\mu_{max}\left(\frac{T}{300}\right)^v - \mu_{min}}{1 + \left(\frac{T}{300}\right)^\xi \left(\frac{N}{N_{ref}}\right)^\alpha}\right] \tag{4.9}$$

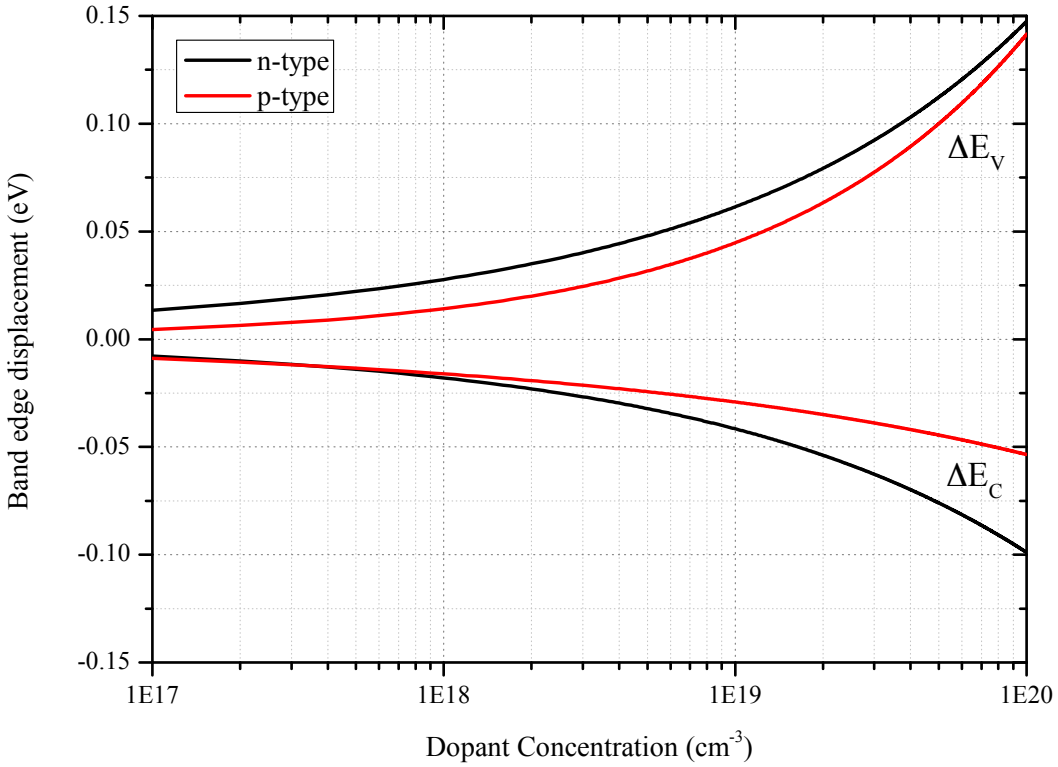


Figure 4.3: Effect of dopant concentration on band edge displacement for n- and p-type 4H-SiC.

where N is the ionised dopant concentration and μ_{min}, μ_{max}, α, v and ξ are fitting parameters. In the Caughey-Thomas model, the parameter μ_{max} represents the carrier mobility of undoped (or unintentionally doped) samples, where the dominant scattering mechanism is the temperature-related lattice scattering,and μ_{min} is the mobility of heavily-doped material, where impurity scattering dominates. N_{ref} is the doping concentration at which the carrier mobility is halfway between μ_{max} and μ_{min} and α is a measure of the rate of transition from μ_{min} and μ_{max}. The parameters v and ξ are used to model the temperature dependence of the carrier mobility.

Due to increasing optical phonon scattering, the carrier drift velocity v_d saturates at high electric fields, and finally reaches a material saturation velocity v_{sat}. Though at low

electric fields the relationship with the carrier drift velocity is linear, it is found that as the carrier velocity approaches υ_{sat} this relationship departs from its linear nature, and the mobility is reduced according to the following model [132]

$$\mu = \frac{\mu_0}{\left[1 + \left(\frac{\mu_0 \mathscr{E}}{\upsilon_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{4.10}$$

where β is an empirical constant that describes the transition between low-field and high-field behaviour. The parameters for carrier mobility modelling are outlined in Table 4.3; these are based on those presented in [103]. The effects of doping concentration and temperature on the electron and hole mobilities in 4H-SiC as described by the above model are illustrated in Figures 4.4 and 4.5; for low doping concentrations, the large mobility asymmetry ratio, b, of 4H-SiC that was discussed in Chapter 3 is clearly evident.

Table 4.3: Carrier mobility model parameters [103].

Parameter	Units	Value	
		Electrons	Holes
μ_{max}	$cm^2/V{\cdot}s$	950	124
μ_{min}	$cm^2/V{\cdot}s$	40	15.9
α	-	0.61	0.34
ν	-	-2.4	-2.15
N_{ref}	cm^{-3}	1.94×10^{17}	1.76×10^{19}
β	-	1	1
υ_{sat}	cm/s	2.2×10^{7}	2.2×10^{7}

As a result of the hexagonal crystal structure of 4H-SiC (and also 6H-SiC), it has been found that the carrier mobility in these materials is anisotropic in nature, which has an impact on the electrical performance of the device. The mobility parameters outlined in Table 4.3 are based on carrier transport along the c-axis of the crystal. As found by Schadt et al. [133], the mobility parallel to the c-axis in 4H-SiC is slightly higher than

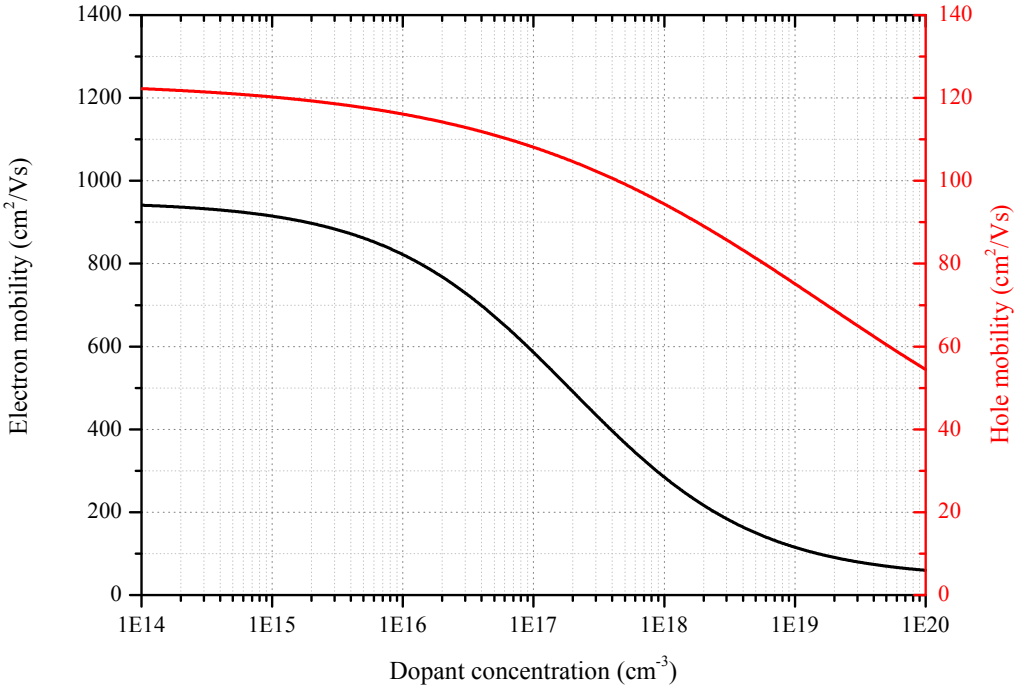


Figure 4.4: Effect of dopant concentration on the electron and hole mobilities in 4H-SiC at 300 K.

that perpendicular to the c-axis, whilst in 6H-SiC the mobility parallel to the c-axis is significantly lower than the mobility perpendicular to the c-axis. Because of this, 4H-SiC is the preferred material for the fabrication of vertical power devices, as the majority of commercially available material is grown slightly off the c-axis (typically 4° or 8°). It is noted that for all numerical simulations carried out in this thesis, an isotropic mobility has been assumed.

4.1.3 Incomplete Ionisation

When compared to Si, it is found that 4H-SiC has the disadvantage (in the context of conventional power device design techniques) of having relatively deep dopant energy levels. Experimental results have shown that typical n-type dopant energy levels are

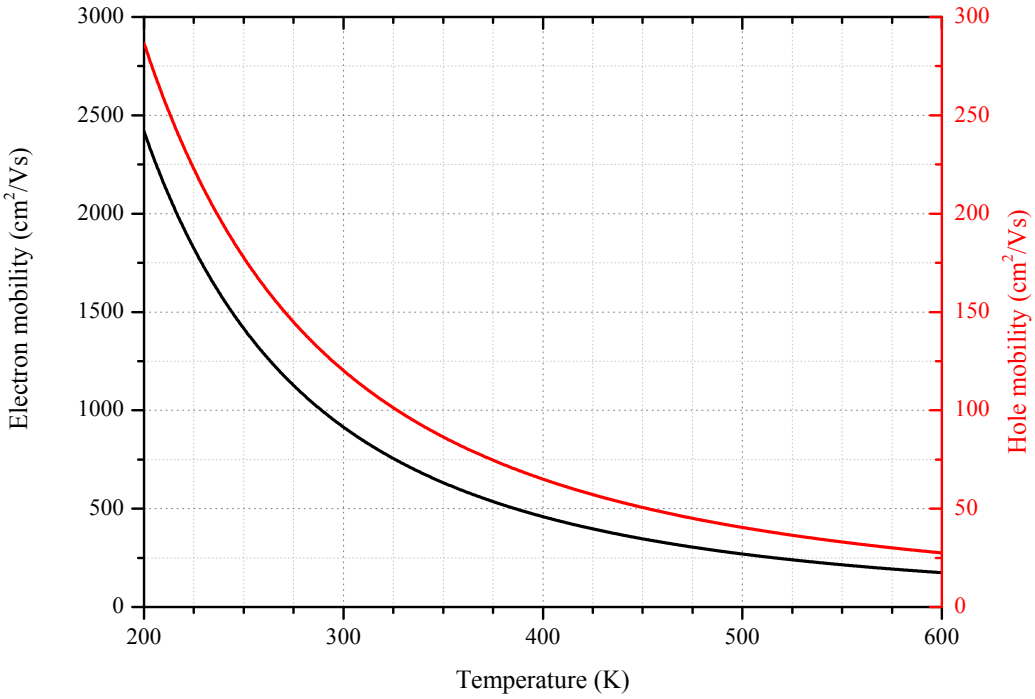


Figure 4.5: Effect of temperature on the electron and hole mobilities in 4H-SiC at a dopant concentration of 10^{15} cm^{-3}.

located approximately 60 meV and 100 meV away from the edge of the conduction band, depending on whether the dopant atom resides on a C- or Si-site [104]. Unfortunately, for bipolar 4H-SiC devices, the situation is worse for p-type dopants, with aluminium and boron being located approximately 220 meV and 330 meV away from the edge of the valence band, respectively [103]. As a result of these large acceptor ionisation energies in 4H-SiC, p-type dopants are in the freeze-out regime at 300 K. For this reason, it is important that incomplete ionisation is accounted for whenever numerically modelling 4H-SiC devices.

The incomplete ionisation model that has been used in this work is widely used, and can be represented by Equations 4.11 and 4.12, for donors and acceptors respectively [42]

$$N_D^+ = \frac{N_D}{1 + GCB \exp\left(\frac{\varepsilon_{F_n} - E_{DB}}{kT_L}\right)} \tag{4.11}$$

$$N_A^- = \frac{N_A}{1 + GVB \exp\left(\frac{E_{AB} - \varepsilon_{F_p}}{kT_L}\right)} \tag{4.12}$$

where N_D and N_A are the total donor and acceptor concentrations, GCB and GVB are the conduction band and valence band degeneracy factors, E_{Fn} and E_{Fp} are the quasi-fermi levels for n- and p-type material, and E_{DB} and E_{AB} are the donor and acceptor energy levels with respect to the conduction and valence band edges.

4.1.4 Carrier Recombination and Generation

In order to simulate the carrier recombination-generation (R-G) processes in the semiconductor, the concentration-dependent SRH [134, 135] and Auger recombination models have been used. Due to the fact that 4H-SiC has an indirect band gap, the effects of direct (or radiative) recombination are considered to be negligible [104], and, as such, are not included in device simulations. Furthermore, because only bulk traps with energy levels close to the intrinsic energy level E_i are effective R-G centres [42], a single trap with an energy level equal to E_i is assumed in the SRH model used in the numerical simulations presented in this thesis. As such, a general expression for the carrier lifetime in 4H-SiC can be written as

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} + S\frac{l}{A} \tag{4.13}$$

As presented in [136], the SRH recombination model can be made a function of doping concentration as described by the following Equation

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p \left[n + n_i \exp\left(\frac{ETRAP}{kT}\right)\right] + \tau_n \left[p + n_i \exp\left(\frac{-ETRAP}{kT}\right)\right]} \tag{4.14}$$

where

$$\tau_n = \frac{TAUN0}{AN + BN\left(\frac{N}{NSRHN}\right) + CN\left(\frac{N}{NSRHN}\right)^{EN}} \tag{4.15}$$

for electrons, and

$$\tau_p = \frac{TAUP0}{AP + BP\left(\frac{P}{NSRHP}\right) + CP\left(\frac{P}{NSRHP}\right)^{EP}} \tag{4.16}$$

for holes. The parameters that have been used for the doping concentration-dependent SRH recombination are based on those in [76] and are outlined in Table 4.4.

Table 4.4: Doping concentration-dependent SRH lifetime model parameters.

Parameter	Units	Value	
		Electrons	Holes
AN, P	-	1	1
BN, P	-	1.95×10^{-3}	1.95×10^{-3}
CN, P	-	4.45×10^{-6}	4.45×10^{-6}
$NSRHN, P$	cm^{-3}	5×10^{15}	5×10^{15}
EN, P	-	2	2

In order to model the Auger recombination within the semiconductor, the following expression is used:

$$\tau_{Auger} = \frac{1}{\gamma_3 n^2} \tag{4.17}$$

where γ_3 is the Auger recombination coefficient and n is the free carrier concentration. The Auger recombination coefficient for 4H-SiC that has been used for the simulations in this work is γ_3=$7\times10^{-31}\mathrm{cm}^6\mathrm{s}^{-1}$; this is based on the value reported by Galeckas et al [85].

4.1.5 Impact Ionisation

As was outlined in Chapter 2, one material property that makes 4H-SiC suitable for high voltage power electronics applications is its ability to withstand very high electric fields, meaning that, compared to Si, 4H-SiC devices can block significantly higher voltages whilst simultaneously offering lower on-resistances. Though semiconductor devices are susceptible to several types of breakdown mechanisms, such as tunnelling breakdown, thermal instability and avalanche breakdown, it is the avalanche breakdown mechanism that imposes an unavoidable physical limit to power semiconductor device designs.

It is found that the impact ionisation coefficients are heavily dependent on the electric field strength in the semiconductor, and are modelled according to Selberherr's model [137]:

$$\alpha_n = a_n \exp\left[-\left(\frac{b_n}{\mathscr{E}}\right)^{\beta_n}\right] \tag{4.18}$$

for electrons, and

$$\alpha_p = a_p \exp\left[-\left(\frac{b_p}{\mathscr{E}}\right)^{\beta_p}\right] \tag{4.19}$$

for holes. The model parameters for impact ionisation in 4H-SiC are based on those experimentally determined by Konstantinov et al. [138] and are outlined in Table 4.5.

Table 4.5: Impact ionisation model parameters.

Parameter	Units	Value
a_n	cm^{-1}	4.08×10^5
b_n	V/cm	1.67×10^7
β_n	-	1.0
a_p	cm^{-1}	1.63×10^7
b_p	V/cm	1.67×10^7
β_p	-	1.0

4.2 4H-SiC PiN Diode Drift Region Design

In the design of high voltage PiN diodes, the first aspect to consider is the specification of the drift region, which is responsible for reverse voltage blocking. Conventionally in 4H-SiC devices, the drift region is realised by growing a thick, lightly-doped epitaxial layer on top of a highly-doped substrate. The design of the drift region is relatively simple, as there are only two key parameters to consider, the doping concentration, N_D, and the drift region thickness, W_D. The goal of the drift region design is to minimise the power dissipation in the device whilst maintaining the required blocking voltage rating when in the off-state.

Based on the one-dimensional parallel-plane junction, analytical solutions for the breakdown voltage, the corresponding depletion width and the critical electric field have been derived for 4H-SiC [43, 69]:

$$BV_{PP} = 4.77 \times 10^{14} N_D^{-5/7} \tag{4.20}$$

$$W_{PP} = 7.15 \times 10^{10} N_D^{-6/7} \tag{4.21}$$

$$\mathscr{E}_{C,PP} = 3.3 \times 10^{4} N_D^{1/8} \tag{4.22}$$

Because of the conductivity modulation effect in power bipolar semiconductor devices, and assuming a sufficiently high carrier lifetime, the background doping concentration of the drift region does not dictate the on-state resistance of the device. As such, the use of a 'punch-through' structure with a thinner, lighter doped epitaxial layer is preferable. In this type of structure the drift region is fully depleted prior to the onset of avalanche, and the electric field distribution is represented as a trapezoidal profile rather than the triangular electric field profile in non-punch-through structures, as illustrated in Figure

4.6. Because the punch-through structure allows a comparable breakdown voltage to be achieved with a thinner drift region than that of a non-punch-through structure, the on-state voltage drop is reduced, and, furthermore, the amount of stored charge is reduced, thus in turn reducing the reverse recovery losses of the device. The punch-through drift region can be designed using the following equation:

$$BV_{PT} = \mathscr{E}_C W_D - \frac{qN_D W_D^2}{2\varepsilon_{SiC}} \tag{4.23}$$

where $\mathscr{E}_C$ is approximated by Equation 4.22.

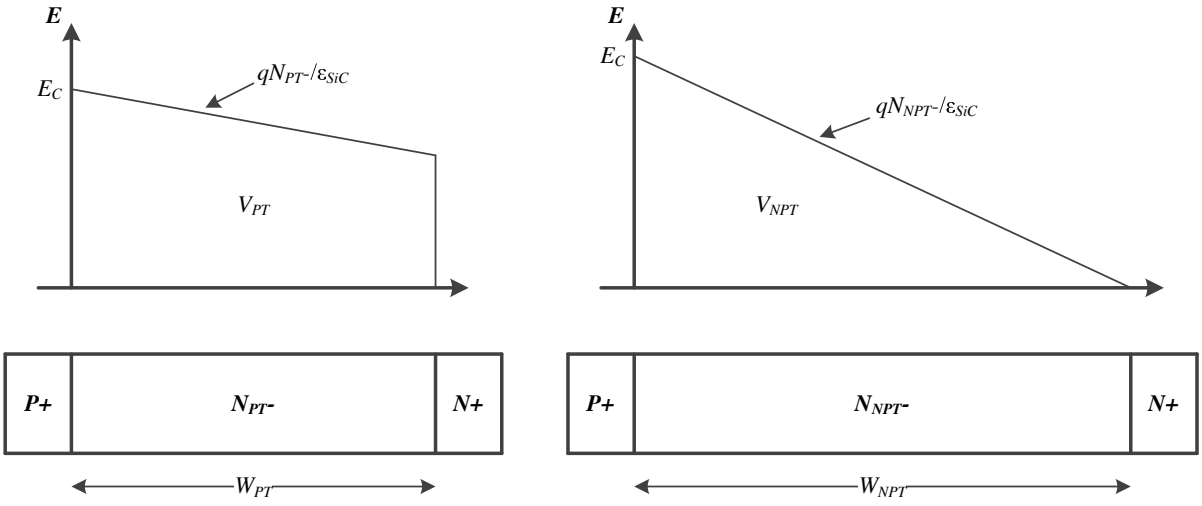


Figure 4.6: Electric field profile at breakdown for punch-through and non-punch-through PiN diode structures.

Based on Equations 4.20 and 4.23, the calculated avalanche limit and punch-through breakdown voltage as a function of doping concentration is shown in Figure 4.7. Based on this ideal parallel-plane case, for an avalanche breakdown voltage of 3.3 kV, a drift region thickness of approximately W_D=25 μm and a doping concentration less than N_D=6×10^{15} cm^{-3} is required. For a 10 kV-rated device, the drift region thickness needs to

be approximately W_D=100 μm and the doping concentration less than N_D=1×10^{15} cm^{-3}. However, in both cases, a slightly punch-through limited structure is achieved by decreasing the doping concentration in the drift region to N_D=2×10^{15} cm^{-3} and N_D=6×10^{14} cm^{-3} for the 3.3 kV- and 10 kV-rated devices respectively, and increasing the drift region thickness to W_D=30 μm (3.3 kV) and W_D=110 μm (10 kV). Using the impact ionisation coefficients outlined in Section 4.1.5, simulated one-dimensional breakdown voltages of BV_{PT}=5.3 kV and BV_{PT}=17.1 kV have been achieved for the 3.3 kV- and 10 kV-rated devices respectively, giving a design margin of up to ∼70% for both device structures.

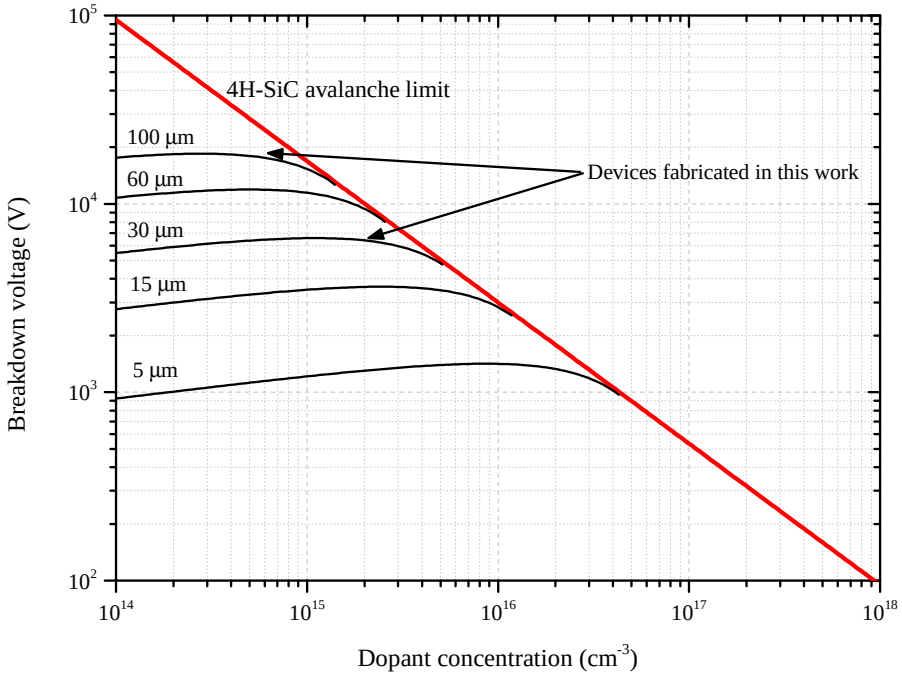


Figure 4.7: Calculated breakdown voltage as a function of doping concentration in 4H-SiC.

4.3 Simulation of the Forward Characteristics of 4H-SiC PiN Diodes

For the high voltage PiN diodes being fabricated in this thesis, the applications for which they are intended to be used in, such as HVDC multi-level converter (MLC) circuits, typically switch at relatively low speeds, of the order several hundred Hertz. As such, the on-state conduction losses, as opposed to the switching losses, are the main contributor to the overall power loss of these devices. It is therefore important that devices being designed in this work are optimised for low on-state losses.

Theoretically, a simple way to tailor the on-state performance of the PiN diode is by varying the high-level carrier lifetime in the drift region of the device. Figures 4.8 and 4.9 show the simulated forward J-V characteristics of the 3.3 kV and 10 kV PiN diodes respectively, with a range of drift region carrier lifetime values. The drift regions of both devices are as outlined in Section 4.2, and a 360 μm thick n-type substrate ($N_D = 1 \times 10^{18}$ cm^{-3}) is used, being representative of the substrates used in practice. In order to ensure sufficient emitter injection efficiency, a 10 μm thick heavily-doped ($N_A = 1 \times 10^{19}$ cm^{-3}) p-type anode is used. By doing this, the effect of carrier lifetime in the drift region on the overall characteristics of the simulated PiN diodes can be independently observed.

It can be seen that for the 3.3 kV-rated PiN diode the improvement in the on-state I(J)-V characteristics saturates at a carrier lifetime of around 500 ns. As this value is within what is achievable in as-grown 4H-SiC material, any post-growth carrier lifetime enhancement treatment is unlikely to yield any improvements in the on-state characteristics of the devices. However, for lower values of carrier lifetime (<50 ns), the excess carrier concentration in the drift region of the diode is insufficient to fully modulate its

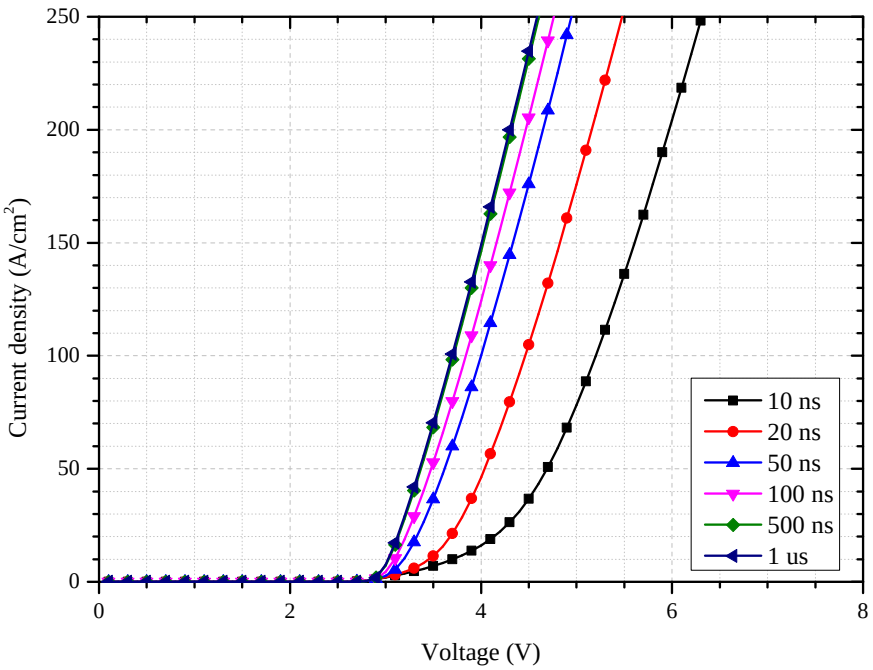


Figure 4.8: Simulated forward J-V characteristics of 3.3 kV PiN diode with varying carrier lifetime at 300 K.

high resistance, leading to a high voltage drop across the device.

The on-state I(J)-V characteristics for the 10 kV-rated PiN diode illustrate that a carrier lifetime of at least 5 μs is required to provide optimum performance, with lifetimes of less than 1 μs leading to significantly worse on-state characteristics. As such, the application of carrier lifetime enhancement treatment is typically necessary to achieve optimum on-state performance for these devices. It is also evident from these simulation results that the turn-on voltage of the diodes is approximately 2-3 V, and is weakly dependent on the carrier lifetime, instead being dictated by the intrinsic carrier concentration of 4H-SiC. This is shown in Figure 4.10, where it is evident that the turn-on voltage increases slightly with increasing carrier lifetime.

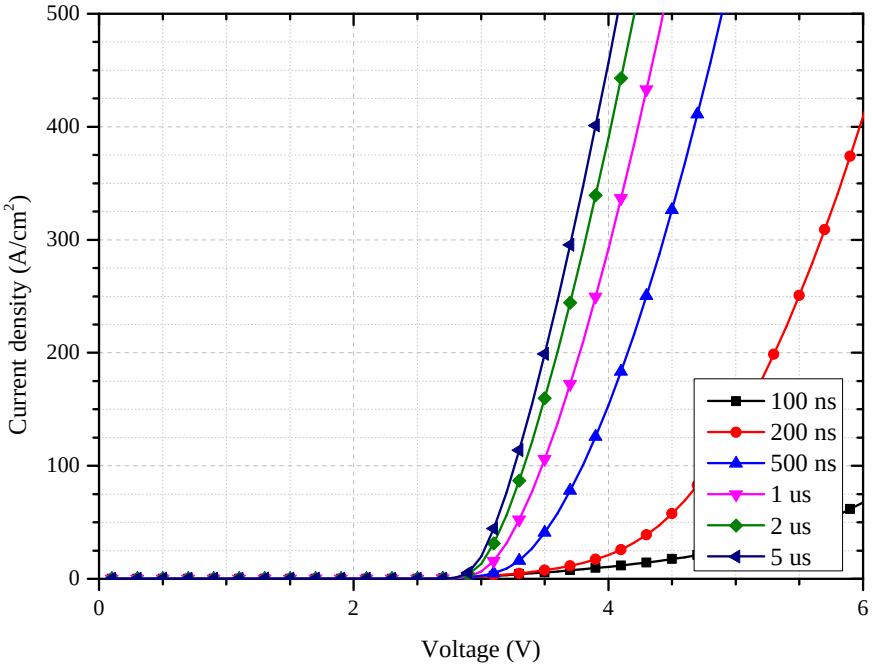


Figure 4.9: Simulated forward J-V characteristics of 10 kV PiN diode with varying carrier lifetime at 300 K.

4.4 High Voltage Edge Termination Design

As discussed in Chapter 3, edge termination is a critical aspect in the design of high voltage power semiconductor devices. As was shown in the previous Chapter, the JTE is a widely applied edge termination technique for high voltage 4H-SiC devices, and has been found to yield breakdown voltages that approach the ideal parallel-plane value with relatively low process complexity. As such, this edge termination technique has been applied to the 4H-SiC PiN diodes designed in this work. In this Section, the design and numerical simulation results of these termination structures are presented, with the best performing structures being selected for incorporation into fabricated devices. It is

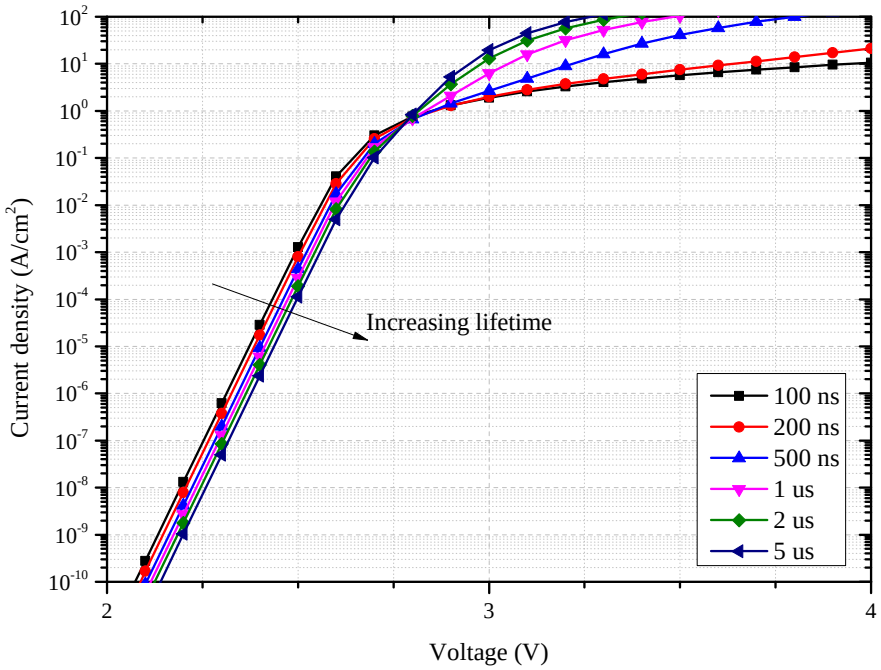


Figure 4.10: Simulated forward log(J)-V characteristics of 10 kV PiN diode with varying carrier lifetime at 300 K.

important to note that unless stated otherwise, simulations were performed assuming zero surface charge. Also, all breakdown voltage values presented from hereon in this Chapter were taken when a current of 1 μA/μm was reached in the device structure.

4.4.1 Numerical Simulation of JTE Structures for 3.3 kV-rated Devices

The first set of numerical simulations for JTE designs have been on PiN diode structures targeting a blocking voltage of 3.3 kV. The basic structure (with the JTE region omitted) used for these simulations is illustrated in Figure 4.11. The doping concentrations of

the $P+$ anode and the $N+$ substrate are $1{\times}10^{19}$ cm^{-3} and $1{\times}10^{18}$ cm^{-3}, respectively. The overall width of the structure is dependent on the width of the JTE region used, and the drift region thickness and doping concentration is as outlined in Section 4.2. As discussed in Section 4.2, the one-dimensional breakdown voltage for the 3 kV-rated device is 5.3 kV; this value is subsequently used as a benchmark for the JTE designs that have been simulated.

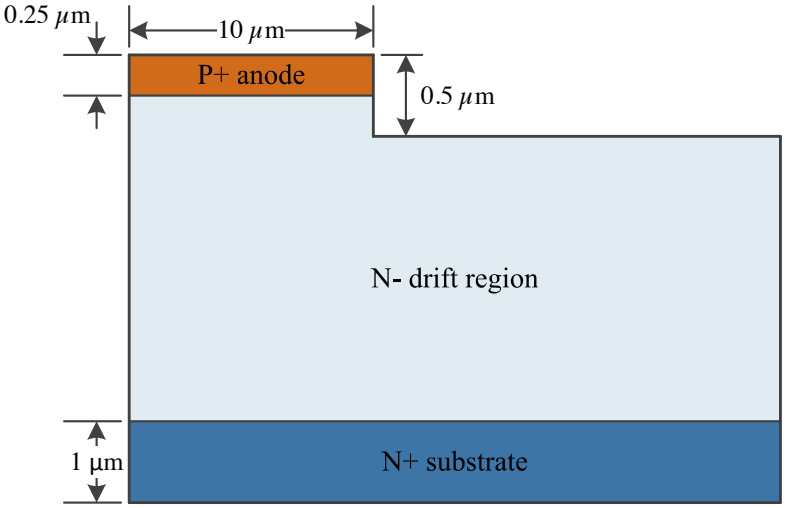


Figure 4.11: Structure of 3.3 kV PiN diode used in reverse breakdown simulations. The drift region thickness has been purposely omitted; this is dependent on the voltage rating for the device.

Prior to simulating the reverse breakdown performance of the PiN diode with JTE structures, a simulation of the basic two-dimensional mesa-isolated PiN diode structure, as illustrated in Figure 4.11, was performed. The simulated electric field distribution for this device at avalanche breakdown is shown in Figure 4.12. This breakdown occurred at a reverse bias of 1280 V; it is evident that, as expected, the breakdown occurs at the mesa sidewall (at 10 μm on the x-axis).

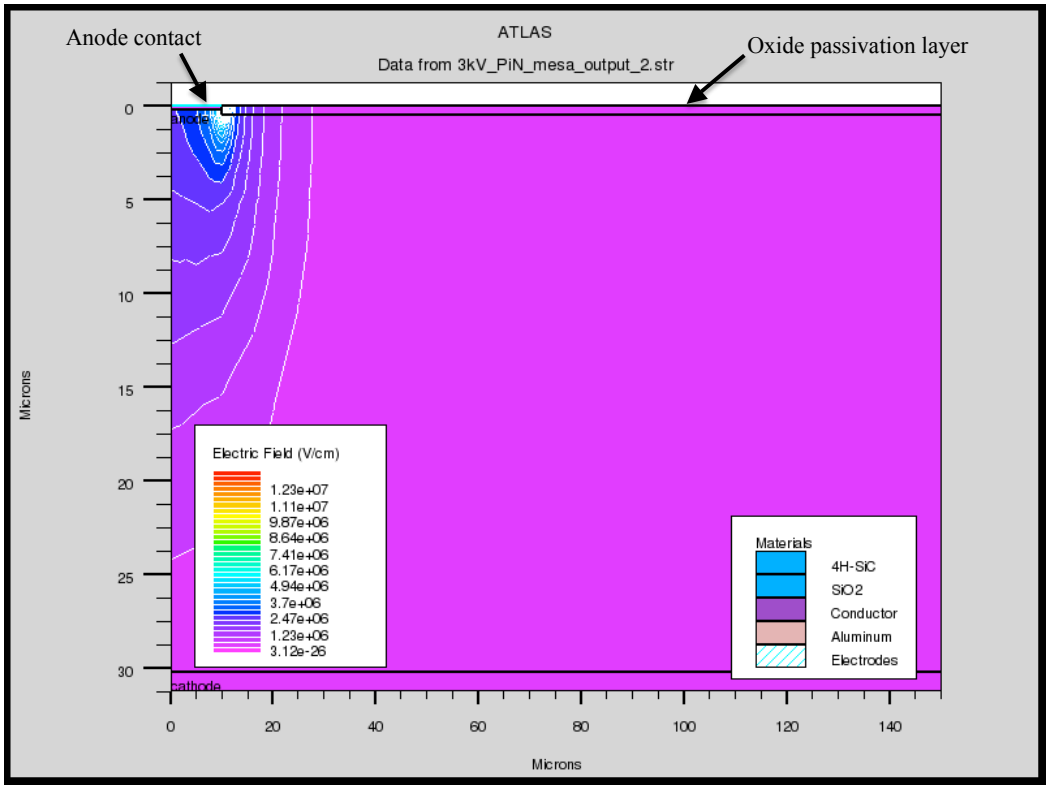


Figure 4.12: Electric field distribution at breakdown in unterminated 3.3 kV mesa-isolated PiN diode.

In order to improve on the reverse breakdown performance of the unterminated device structure, PiN diodes with a single-zone JTE (SZ-JTE) were simulated. In these simulations, the JTE width W_{JTE} and JTE doping concentration $N_{A,JTE}$ were varied to determine the optimum parameters. A 700 nm deep box profile with a Gaussian tail has been used to represent the implanted JTE region. The results of these simulations are shown in Figure 4.13. The first observation that is made from these results is that increasing the width of the JTE region to more than twice the width of the drift region has a minimal effect on the breakdown performance of the device. The second observation made is that the sensitivity of the achievable breakdown voltage to the doping concentration of the JTE region is very high; for a JTE width of 60 μm, the breakdown

voltage decreases from its peak value of 4086 V at $N_{A,JTE}$=1.1×10^{17} cm^{-3} to 1582 V at $N_{A,JTE}$=1.5×10^{17} cm^{-3}. This corresponds to a drop of ∼60% in the achievable breakdown voltage for an increase in JTE doping concentration of ∼25%. For the practical fabrication of high voltage power devices this high sensitivity of the breakdown voltage to the JTE doping concentration is undesirable; as such, different JTE structures that aim to reduce this sensitivity have been investigated.

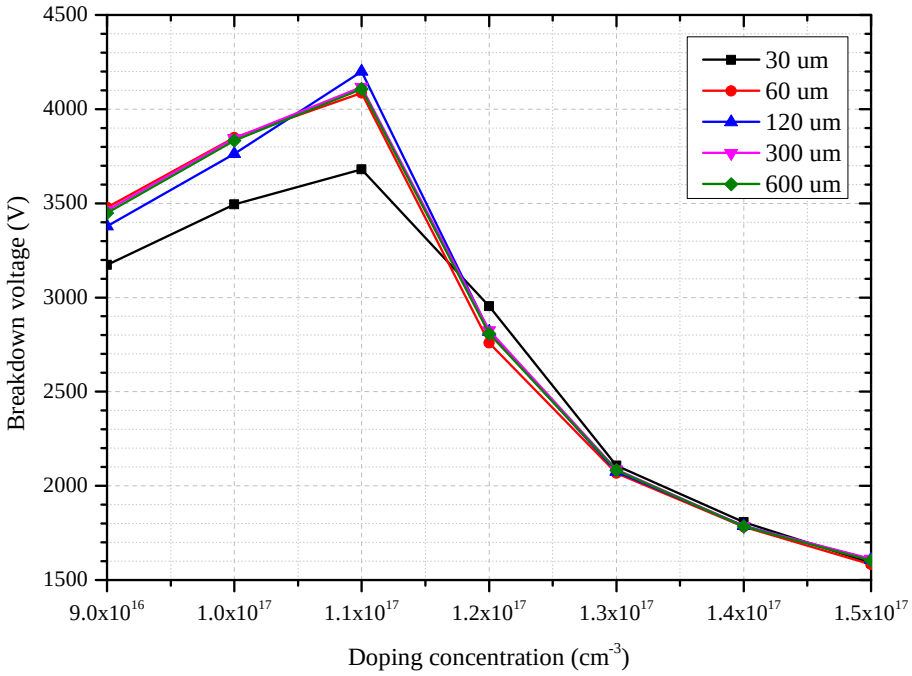


Figure 4.13: Breakdown voltage versus JTE doping concentration for 3.3 kV SZ-JTE structures of varying JTE width.

As presented in the literature [60, 81, 139], an effective, proven method of terminating high voltage 4H-SiC power devices is to use the "space-modulated" JTE technique, illustrated in Figure 3.15. Compared to other methods used to form JTE regions for high

voltage devices, this method has the advantage of being simple to fabricate, requiring only basic mask patterning and etching processes, and can be formed with a single ion implantation stage (although the use of a second implantation stage has been shown to further reduce the sensitivity to implant dose). As such, employing this JTE technique is beneficial for minimising the overall device processing complexity and cost.

In order to investigate the effectiveness of the SM-JTE technique, a range of these termination structures integrated into the mesa anode PiN diode design have been numerically simulated. With the SM-JTE structures, the only design constraint is the lateral spacings between the implanted regions; a minimum spacing of 6 μm was used as this is comfortably within the capability of the photolithography equipment in the semiconductor cleanroom facility used to fabricate the devices. Figure 4.14 shows the simulated breakdown voltage characteristics as a function of the doping concentration of the implanted JTE region, for a range of SM-JTE structures. The SM-JTE design is illustrated in Figure 4.15, and the dimensions of each structure that has been investigated are outlined in Table 4.6. It can be seen that by increasing the number of implanted zones in the SM-JTE structure, the sensitivity to the doping concentration is reduced and the maximum breakdown voltage is increased, when compared to the simulated characteristics of the SZ-JTE structure. For the 6Z-SM-JTE structure, the maximum breakdown voltage is 4970 V, which is ∼94% of the one-dimensional parallel-plane value, giving a design margin of ∼50% on the targeted blocking voltage of 3.3 kV. The electric field distribution at breakdown in the PiN diode with the 6Z-SM-JTE structure (N_A =1.4×10^{17} cm^{-3}) is shown in Figure 4.16. It can be seen that the presence of the space-modulated rings towards the periphery of the device progressively reduce the electric field near the 4H-SiC/SiO_2 surface, which allows a high reverse voltage to be attained.

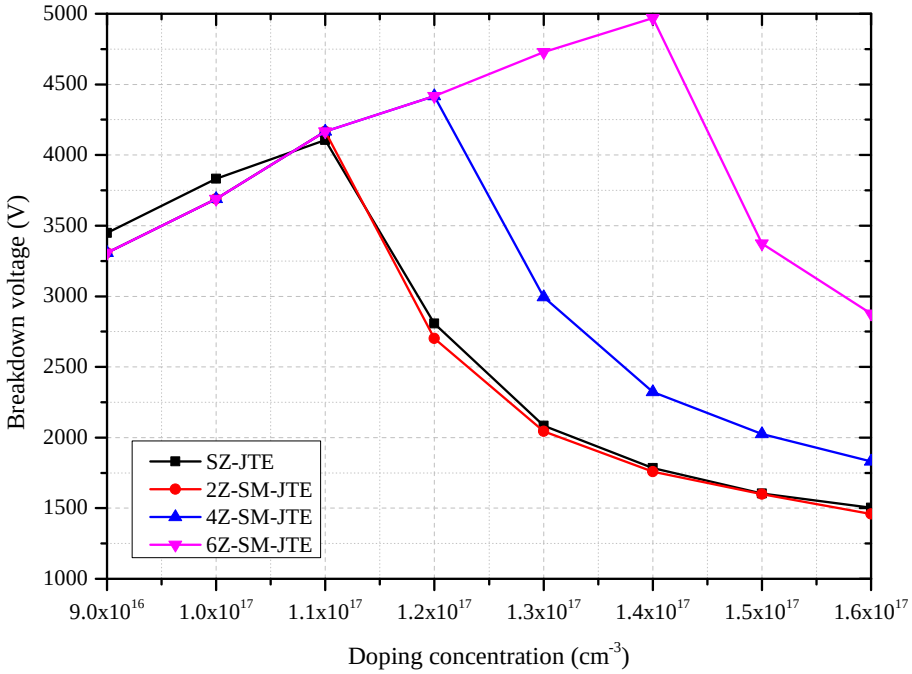


Figure 4.14: Breakdown voltage versus JTE doping concentration for 3.3 kV SM-JTE structures with a range of implanted zones. For comparison, the breakdown voltage characteristics of the SZ-JTE structure are also shown.

In practice, the reduced sensitivity to JTE doping concentration is crucial, as the breakdown characteristics of 4H-SiC PiN diodes are severely affected by the presence of charge near the SiO_2/4H-SiC interface. This still remains one of the most problematic

Table 4.6: Dimensions of SM-JTE designs. Design parameters refer to those in Figure 4.15 (all dimensions in μm). The total JTE width in each of the designs is 600 μm, with the large JTE region being 500 μm wide.

Design ref.	s_1	z_1	s_2	z_2	s_3	z_3	s_4	z_4	s_5	z_5
2Z-SM-JTE	20	80	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
4Z-SM-JTE	10	22	16	16	22	14	n/a	n/a	n/a	n/a
6Z-SM-JTE	6	14	8	12	10	10	12	8	14	6

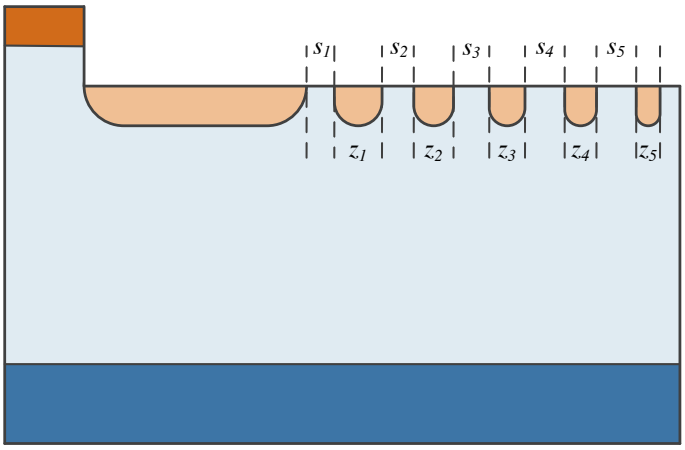


Figure 4.15: Schematic of SM-JTE structure in a mesa anode PiN diode. The structure shown here is for a 6Z-SM-JTE design (not to scale).

issues in the processing of 4H-SiC devices; in comparison with Si semiconductor technology, the measured fixed oxide charge and interface state density of 4H-SIC MOS-based devices is much higher, being of the order 10^{12} cm^{-2} [140]. Moreover, the magnitude of this charge will change depending on the passivation conditions and may also vary across the same epiwafer.

To demonstrate the impact that a poor quality SiO_2/4H-SiC interface has on the performance of a PiN diode with the SM-JTE structure, the reverse breakdown characteristics have been simulated with an oxide charge present. These simulation results are shown in Figure 4.17. It can be seen that the presence of oxide charge causes a shift in the reverse breakdown voltage against JTE doping concentration profile; a positive oxide charge results in the peak of the curve being shifted towards heavier JTE doping and a negative oxide charge shifts the peak of the curve towards lighter JTE doping.

The cause of this shift in the reverse breakdown performance of the PiN diode due to oxide charge is explained with the aid of Figure 4.18. When a positive oxide charge exists, the negative charge of the ionised acceptors within the JTE region is partially com-

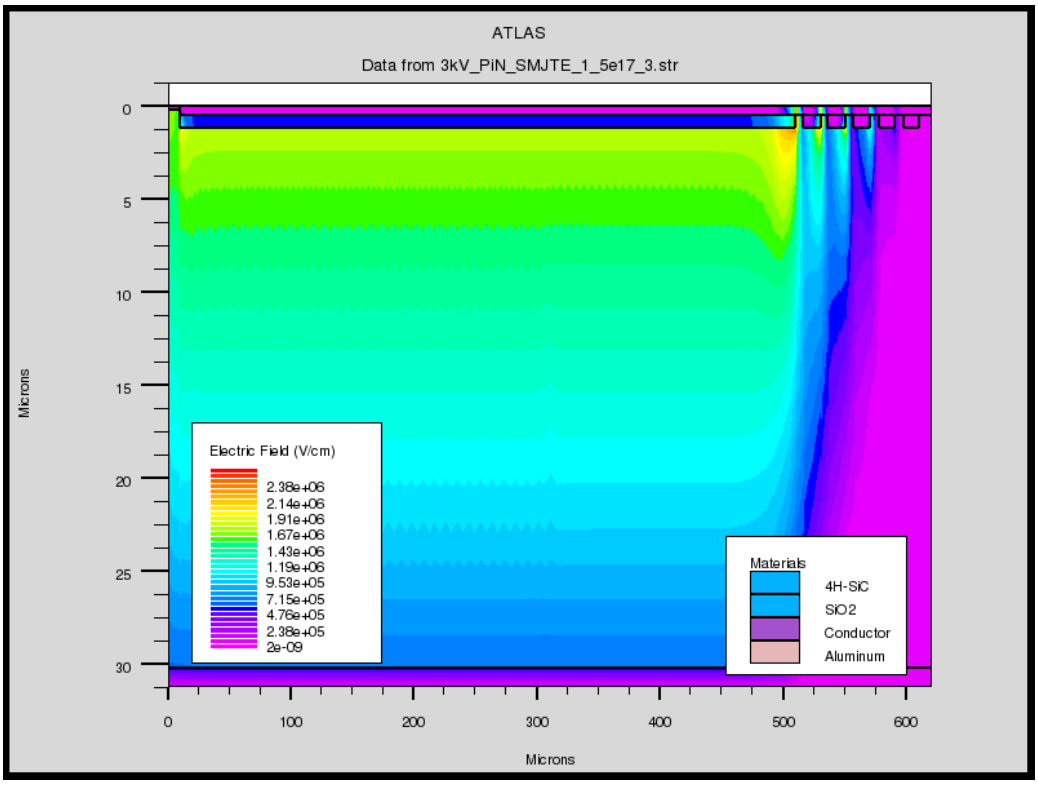


Figure 4.16: Electric field distribution at breakdown for 3.3 kV 6Z-SM-JTE structure (N_A =1.4×10^{17} cm^{-3}).

pensated, thus reducing the net concentration that are available for the lateral spreading of the electric field. As such, a higher JTE doping concentration is required to obtain the maximum achievable breakdown voltage. When a negative oxide charge exists, this adds to the negative charge of the ionised acceptors in the JTE region, increasing the net concentration that are available for electric field spreading. This means that a lower JTE doping concentration is required to achieve the maximum breakdown voltage. In order to minimise the impact of oxide charge on the reverse breakdown performance of the 4H-SiC PiN diode, the oxide charge should be small in comparison to the total JTE dose, such that $Q_{ox} \ll 10^{13}$ cm^{-2}.

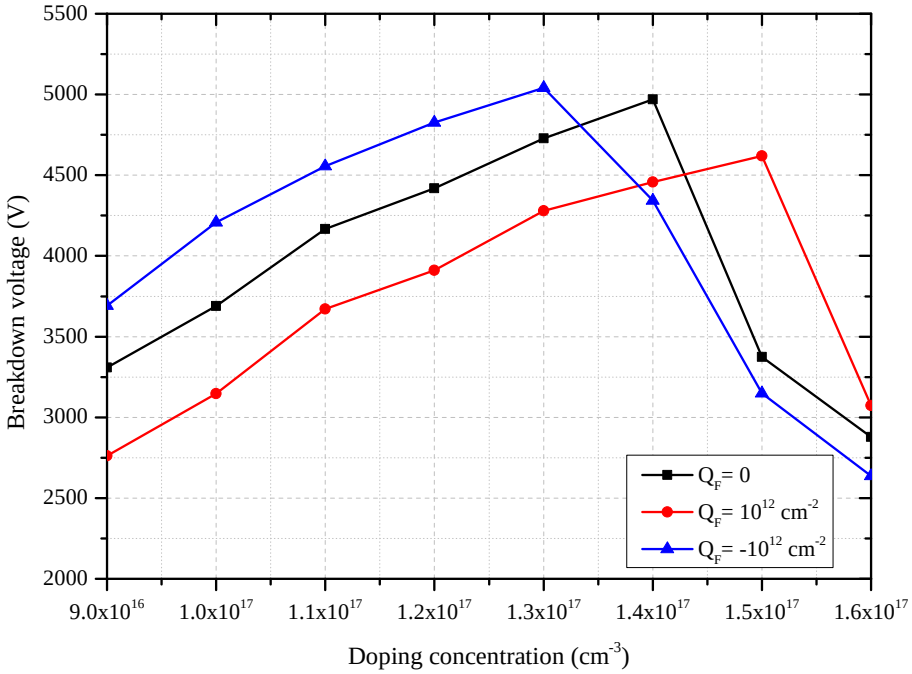


Figure 4.17: Effect of oxide charge on the breakdown voltage versus JTE doping concentration for 3.3 kV 6Z-SM-JTE structure.

4.4.2 Numerical Simulation of JTE Structures for 10 kV-rated Devices

Following the numerical simulation of edge termination structures for the 3.3 kV-rated PiN diodes, the next set of simulations, presented in this Section, are those for the 10 kV-rated PiN diodes. The dimensions of the basic structure used for simulations are outlined in Figure 4.11, and the drift region design is as specified in Section 4.2. This drift region design yields a one-dimensional parallel-plane breakdown voltage of 17.1 kV, and the simulated breakdown voltage of the two-dimensional mesa-isolated PiN diode with no termination was found to be 1745 V.

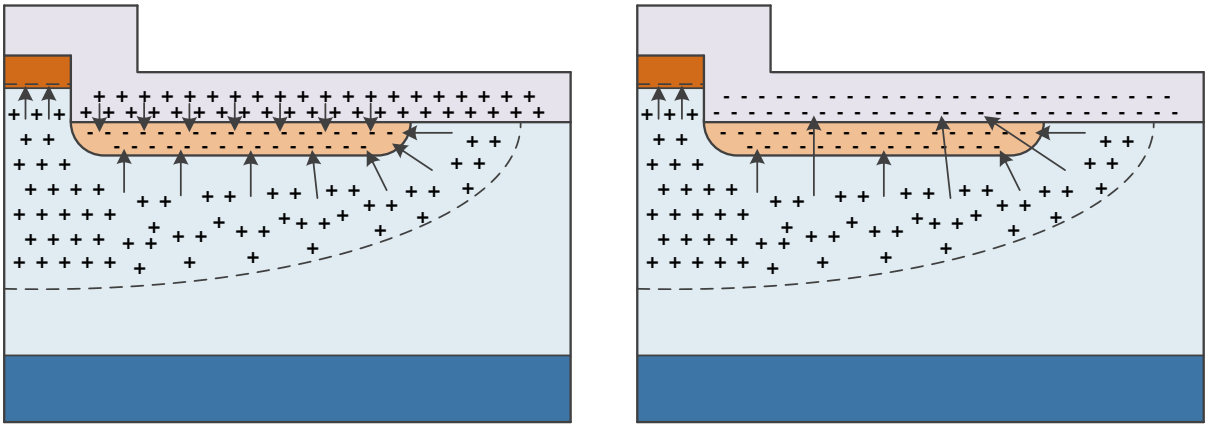


Figure 4.18: Schematic of JTE structure with positive (left) and negative (right) oxide charge under reverse bias conditions.

As with the 3.3 kV-rated PiN diodes, SZ-JTE structures have first been simulated for the 10 kV-rated devices, across a range of doping concentrations. Following this, the reverse breakdown performance of the 6Z-SM-JTE (with a total width of 600 μm) was simulated. The results for both of these sets of simulations are shown in Figure 4.19. It is evident that unlike with the 3.3 kV-rated device reverse breakdown simulations where the use of the SM-JTE structure provided improved breakdown performance, the use of the SM-JTE has a negative impact on the reverse breakdown performance of the 10 kV-rated PiN diode when compared to a SZ-JTE with equivalent total width. The lateral electric field distributions in the SZ-JTE and 6Z-SM-JTE devices along the plane of the $P+/N-$ junction are shown in Figure 4.20 and 4.21 respectively. Both electric field distributions shown were taken at the point of reverse breakdown with a JTE doping concentration of 1.3×10^{17} cm^{-3}, which is the optimum doping concentration for the SZ-JTE structure.

It can be seen from Figure 4.20 that the point of breakdown occurs at the mesa side of the JTE in the device with the SZ-JTE structure, whilst the device with the 6Z-SM-JTE structure breaks down at the far edge of the 500 μm wide JTE region (shown in Figure

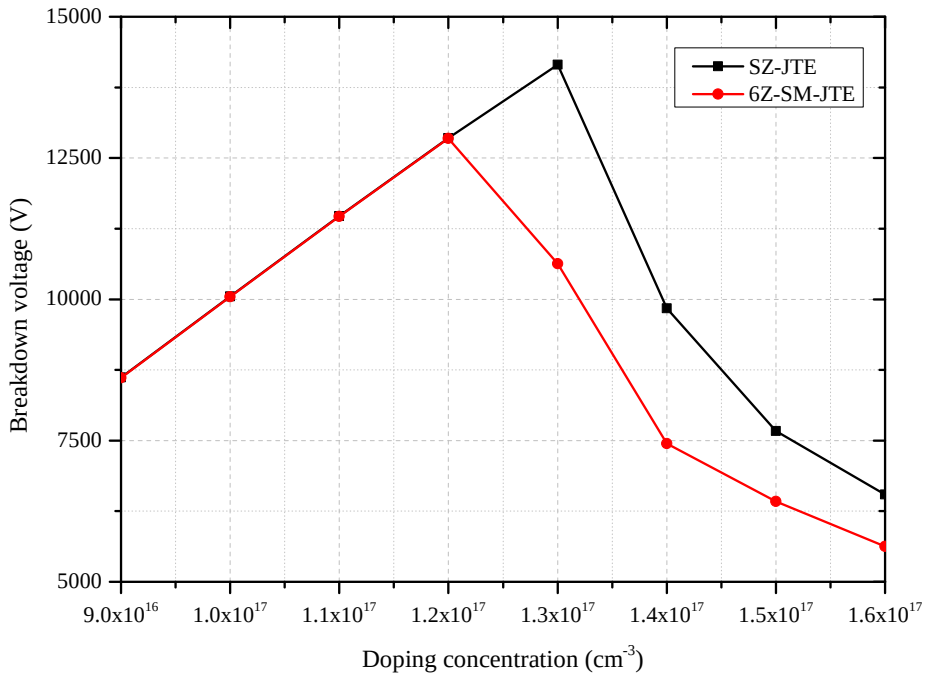


Figure 4.19: Breakdown voltage versus JTE doping concentration for 10 kV SZ-JTE and 6Z-SM-JTE structures.

4.21). This suggests that the 500 μm wide JTE region is not wide enough to spread the electric field sufficiently to prevent the high field crowding at the far edge of this implanted region, and the outer implanted rings are too far away from the main JTE region to spread the electric field sufficiently. The fact that the breakdown occurs at the far edge of the main JTE region highlights the fact that the JTE doping is too high; however, by lowering the doping it was found that the breakdown voltage of the device dramatically decreases, illustrating the high sensitivity of the JTE structure in this device. Because it is undesirable to increase the total width of the JTE region, other methods of minimising the electric field crowding have been investigated. As was reported in [76], the use of multiple-zone JTE structures have been shown to be effective for blocking high

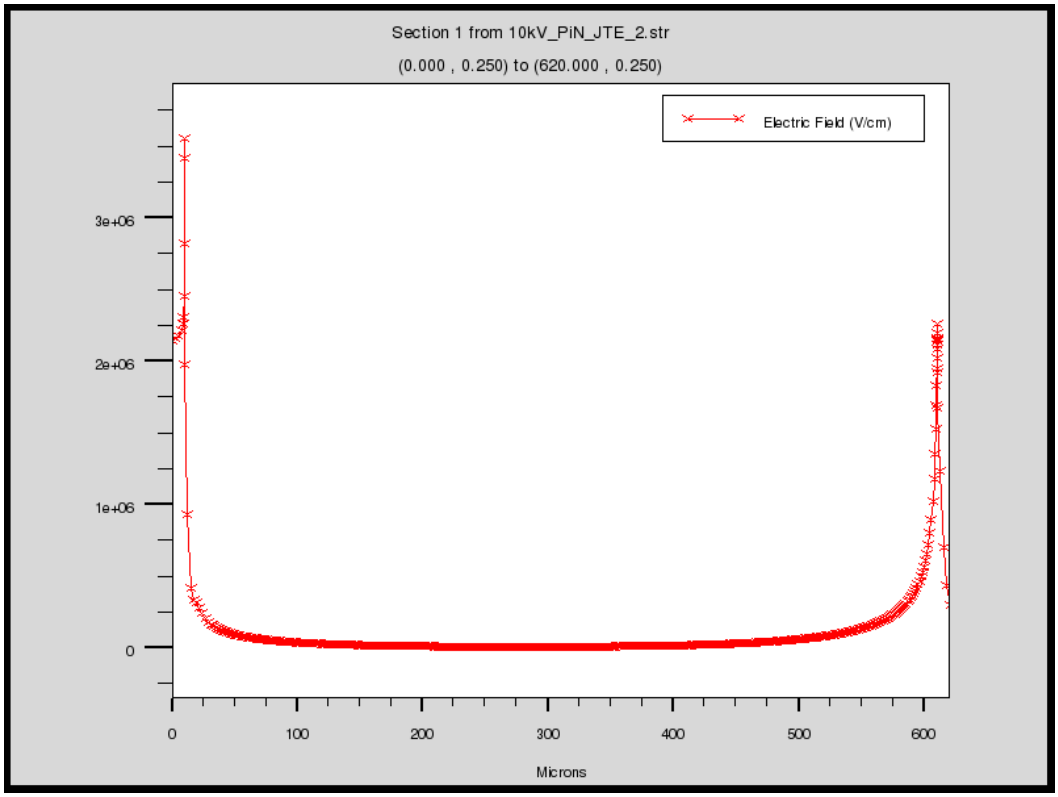


Figure 4.20: Lateral electric field distribution of 10 kV PiN diode with SZ-JTE structure.

voltages in 4H-SiC power devices, though, as discussed in Chapter 3, are typically more complex to fabricate than the SM-JTE structures previously outlined. The simulation results for a range of MZ-JTE structures for 10 kV PiN diodes are illustrated in Figure 4.22 and Figure 4.23, which show the simulated breakdown characteristics for dual- and quad-zone JTE structures respectively. In both sets of simulations, the ratio of doping concentration across the zones has been varied to determine the optimum parameters for achieving high breakdown voltage and low sensitivity to JTE doping concentration.

The first MZ-JTE structures that have been investigated were based on a dual-zone JTE topology, with each zone being 300 μm wide. It can be seen from Figure 4.22 that the use of dual-zone JTE structures offers performance advantages when compared to the

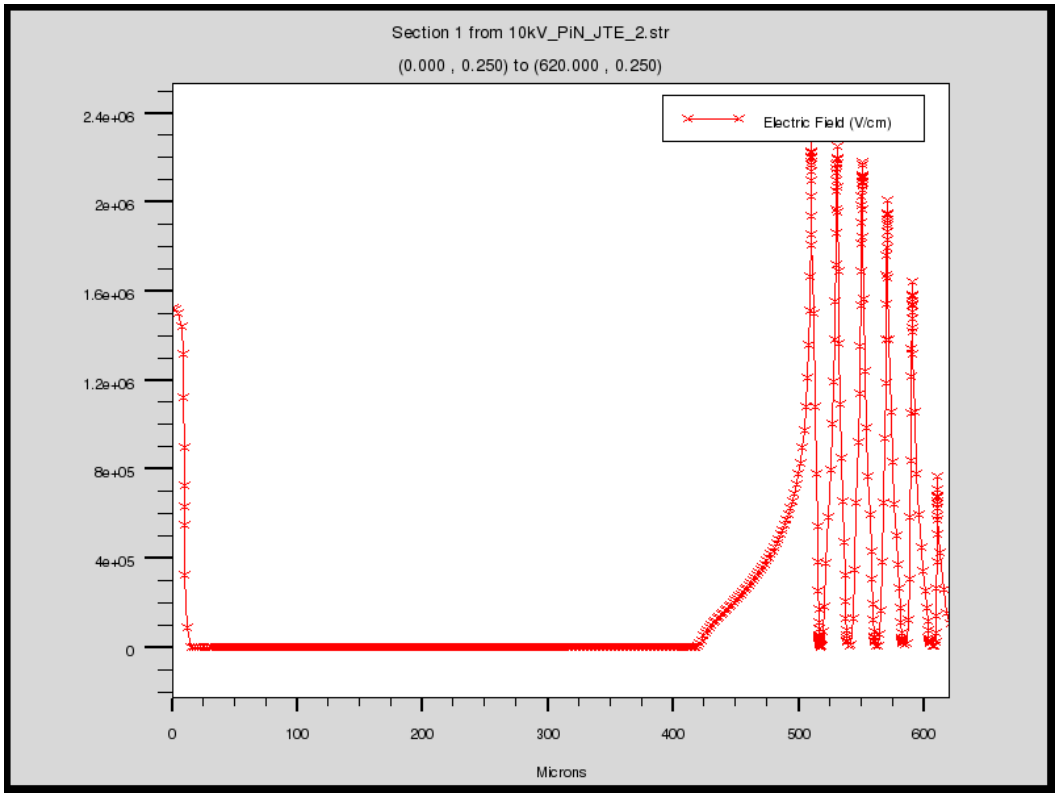


Figure 4.21: Lateral electric field distribution of 10 kV PiN diode with 6Z-SM-JTE structure.

SZ-JTE, in terms of both achievable breakdown voltage and sensitivity to the JTE doping concentration. However, the breakdown voltage performance of the dual-zone (DZ) JTE structure is heavily dependent on the ratio of doping concentration across the JTE zones; these simulations have indicated that using a ratio of 2:1 offers the lowest sensitivity to implant doping concentration. By using a quad-zone (QZ) JTE (with each zone being 150 μm wide), the reverse breakdown performance of the PiN diode can be further enhanced compared to that of the DZ-JTE design. This is illustrated in Figure 4.23. It is evident from these simulation results that the sensitivity to JTE doping concentration is vastly reduced when compared to the optimum DZ-JTE design.

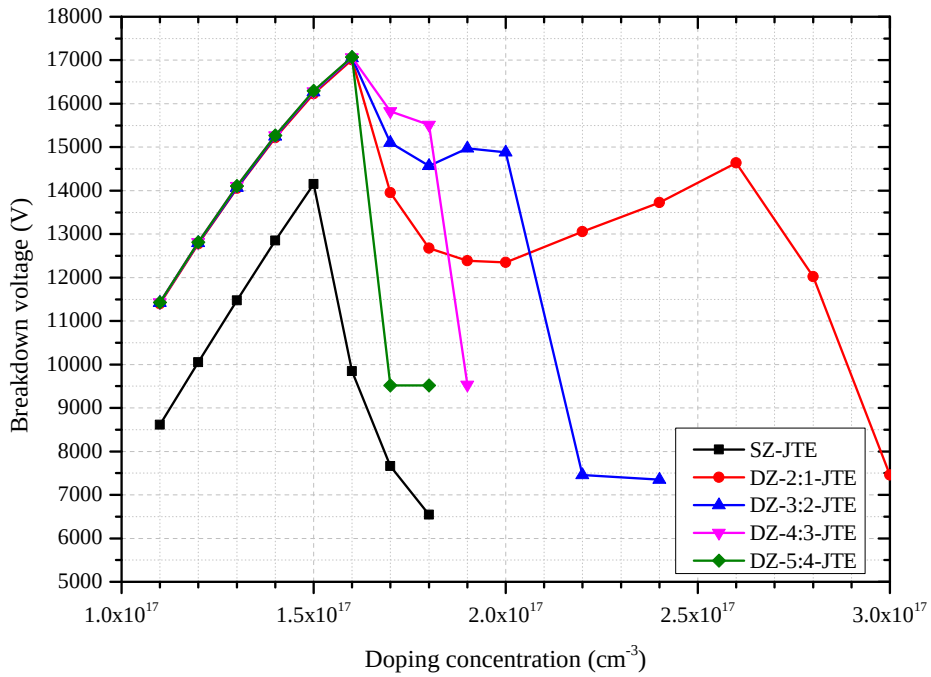


Figure 4.22: Breakdown voltage versus JTE doping concentration for 10 kV SZ-JTE and dual-zone JTE structures.

Although these numerical simulations of multi-zone JTE designs have yielded good results in terms of their reverse breakdown voltage performance, it is evident that the formation of this type of structure in practice is considerably more complex than that of the SZ-JTE or the SM-JTE, which both require just a single photolithography, etching and implantation fabrication stage. In [76], a multiple oxide deposition and etch process was employed, which resulted in a graded JTE structure with decreasing doping concentration away from the mesa periphery. However, this process required four separate photolithography, oxide mask deposition and etching processes, followed by a single implantation process, and hence is both time consuming and complex. A simpler method to obtain a graded JTE structure is suggested in [69], whereby a mask with decreasing window area

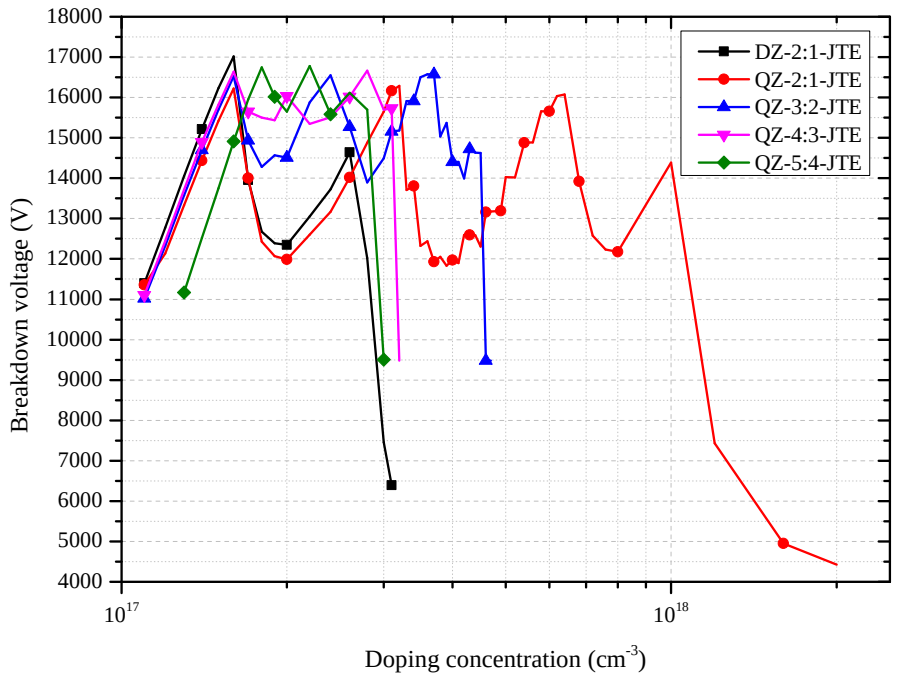


Figure 4.23: Breakdown voltage versus JTE doping concentration for 10 kV quad-zone JTE structures (results for optimum dual-zone JTE structure are also shown, for comparison).

is used to obtain the required graded JTE structure. An example of the layout of such a mask is shown in Figure 4.24, in which the device anode is represented by the circular feature in the centre of the Figure, and the blue shaded regions which increase in area moving away from the anode represent the JTE implant mask. By taking advantage of the fact that boron diffuses in 4H-SiC during high temperature annealing processes [141] and carefully controlling the annealing parameters, the boron will diffuse sideways between the masked areas in the 4H-SiC, resulting in a JTE with a lateral tapered doping profile.

It has been previously reported that premature breakdown can occur at the mesa-etched anode sidewall, due to the poor morphology of the etched surface, in addition

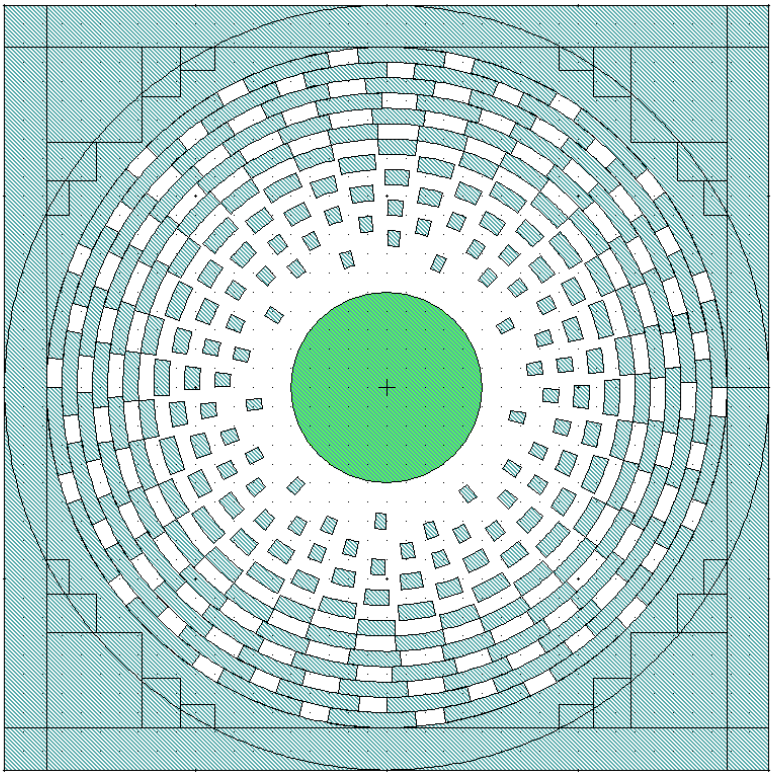


Figure 4.24: Masking layout for quad-zone JTE structure. The shaded regions are where the photomask would block the implant from penetrating the 4H-SiC. It is noted that this mask design has only been designed for 10 kV-rated devices.

to the sharp corner at the foot of the etched sidewall [76]. One method to alleviate this problem is to use a bevelled mesa structure, as described in [80]. However, this structure is complex to achieve in practice, relying on tightly controlled, optimised etching conditions. Because the problem of premature breakdown at the mesa sidewall relates to the surface quality, electric field crowding can be prevented at the sidewall surface by incorporating a shallow, highly doped implanted region in addition to the lateral JTE region. In practice, this implanted region, from hereon referred to as the "sidewall implant", can be achieved by implanting the dopant species at an angle, and rotating the sample during the implantation process (for example, in 60° segments) to ensure full

coverage on the cylindrical mesa structure. Due to the need for a highly doped implanted region, and because only a shallow implant depth is required, Al is the most suitable dopant species for this application. Figure 4.25 shows the simulation results for a QZ-JTE structure with and without the sidewall implant. Due to the improvement in reverse breakdown performance at low JTE doping concentrations, it is evident that the sidewall implant is effective in preventing breakdown at the mesa periphery, thus further reducing the sensitivity to JTE doping concentration for high voltage 4H-SiC PiN diodes. Though not shown in this Figure, it was verified that the breakdown performance at higher JTE doses was unaffected by the presence of the sidewall implant.

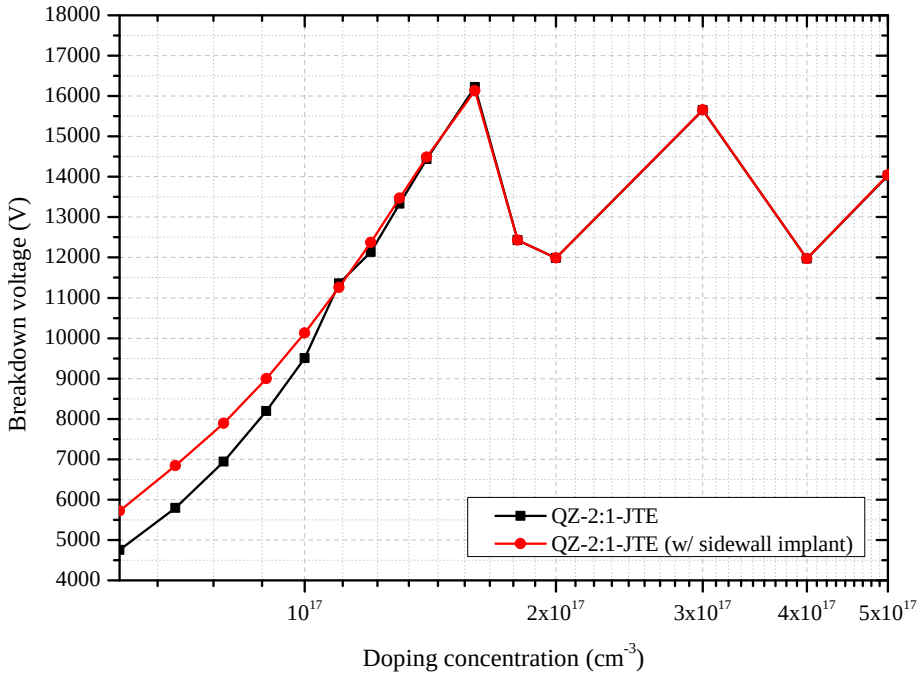


Figure 4.25: Breakdown voltage versus JTE doping concentration for 10 kV quad-zone JTE structure with and without sidewall implant.

4.5 Summary

In this Chapter, the design of high voltage 4H-SiC PiN diodes has been presented. The physical models and their respective numerical parameters were first outlined; these formed the basis of the subsequent modelling work carried out. Next, the device designs were presented, the first element of which was the drift region design for both 3.3 kV and 10 kV devices. The drift regions of both types of device were designed to obtain a punch-through structure, which, by allowing a thinner drift region, requires a lower carrier lifetime for optimum conductivity modulation, and thus also results in lower switching losses than non-punch-through structures. Following this, numerical simulations of the forward characteristics of the devices were performed, highlighting the dependence of low on-state losses on the minority carrier lifetime in the semiconductor. These simulations confirmed that lifetimes of 500 ns and 5 μs were required for optimum on-state performance of 3.3 kV and 10 kV PiN diodes respectively.

Crucial to the design of high voltage power semiconductor devices, edge termination structures for the 3.3 kV and 10 kV PiN diodes were also simulated. It was found that for the 3.3 kV devices, the SM-JTE structure was effective in achieving a breakdown voltage that was nearly 95% of the one-dimensional parallel-plane voltage, whilst also offering reduced sensitivity to the implant doping concentration compared to the conventional SZ-JTE structure. However, this wasn't the case for the 10 kV devices, which were found to require a multiple-zone JTE structure to achieve reverse breakdown performance that surpassed that for the conventional SZ-JTE structure. The use of a QZ-JTE structure was demonstrated to offer markedly improved characteristics over the SZ-JTE and DZ-JTE structures, and suggestions for how the QZ-JTE structure can be realised with a simple fabrication process were outlined. Finally, simulation results illustrated that the use of a

mesa sidewall implant could further enhance the reverse breakdown performance of 10 kV PiN diodes, and a fabrication process for realising this structure was proposed.

Chapter

5 Characterisation Techniques for High Voltage 4H-SiC PiN Diodes

In this Chapter the characterisation techniques that are to be applied to the high voltage 4H-SiC PiN diodes fabricated in this work are discussed. The electrical characterisation techniques are first discussed; these include methods to evaluate the on-state characteristics, reverse blocking and switching behaviour of the PiN diodes, as well as the measurement of contact resistance. In addition, the methodology for extracting the carrier lifetime of the devices from reverse recovery characteristics is outlined. Following this, the physical characterisation methods that have been applied in this work are discussed.

5.1 Electrical Characterisation

5.1.1 Forward I-V Measurements

The most fundamental, yet very powerful, semiconductor device analysis tool is the current-voltage (I-V) measurement, which, in the case of the forward-biased PiN diode, can provide the reverse saturation current, the ideality factor and the on-resistance of the

device. Low-current (up to 100 mA) measurements have been performed at the University of Warwick using an Agilent Technologies B1500A Semiconductor Parameter Analyser in conjunction with a four-point probe station. High-current (up to 1 A) measurements have been performed at Cambridge University using a Keithley 4200-SCS Semiconductor Parameter Analyser in conjunction with a four-probe station, and a Tektronix 371B high power curve tracer in conjunction with a custom-designed two-probe station. Each of these test setups also allowed on-die measurements to be made at temperatures between 25°C and 300°C. To avoid self-heating of the devices under test, pulsed power mode has been used when performing forward I-V measurements. In each of these test setups, the probe station has been configured for measurement of vertical devices, and where four probes were used, two probes were used for force and two for sense, to prevent the probe resistance affecting the results.

5.1.2 Reverse Breakdown Characterisation

Although it is essentially another I-V measurement, the reverse breakdown measurement differs in that, for the devices fabricated in this work, the voltages are significantly higher than those dealt with for forward I-V measurements, and the current levels are significantly lower. As such, a custom-designed measurement setup has been developed and used. This was based on a HPp-200-756 (ETPS Limited) 20 kV/75 mA power supply unit to provide the device test voltage; this power supply is controlled via USB from LabView. The voltage across the device under test, as well as the current flowing through the device, are also monitored in LabView. The calibration results for this test rig are shown in Figure 5.1. This Figure shows that the reverse breakdown voltages of a range of devices measured using the custom-designed test rig are comparable to those achieved with the Tektronix

371B curve tracer (which has a maximum voltage output of 3 kV). It is also evident that the custom-designed test rig has higher current resolution than the curve tracer, thus offering a more accurate visualisation of the low-current device characteristics prior to breakdown.

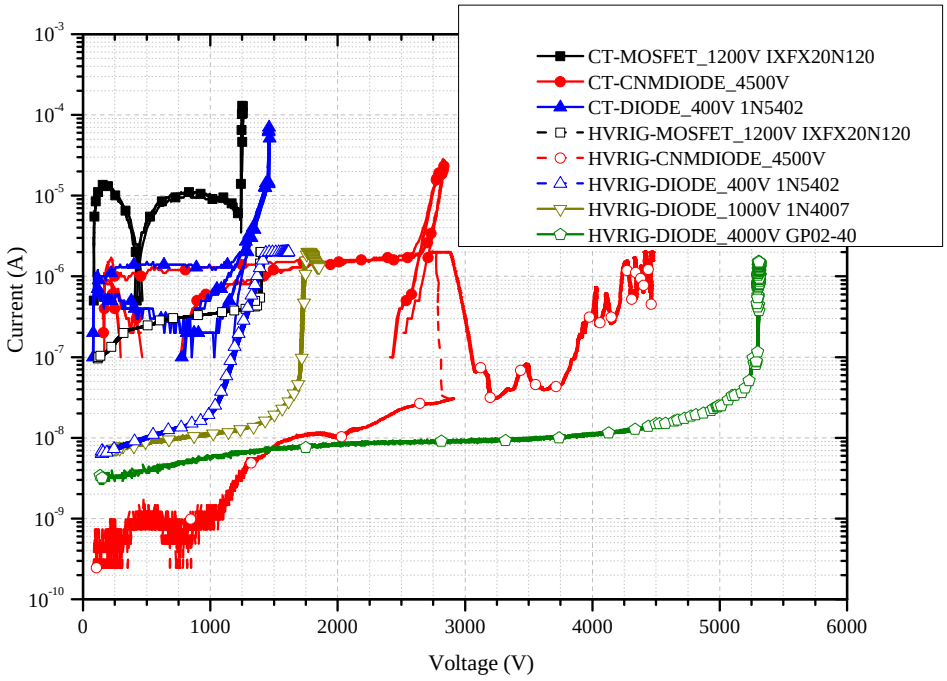


Figure 5.1: Calibration results for the high voltage reverse breakdown test rig. The solid trace / solid marker characteristics were measured on the Tektronix 371B curve tracer; the dashed trace / hollow marker characteristics were measured on the high voltage reverse breakdown test rig.

5.1.3 High Voltage Inductive Switching Characterisation

In order to evaluate the switching performance of the fabricated diodes, a custom-designed clamped inductive switching test rig has been developed as part of this project; this is

shown schematically in Figure 5.2 and is illustrated in Figure 5.3. In this circuit, a 12 kV/125 mA capacitor charger power supply unit (the LPp-120-137 by ETPS Limited) is used to charge up an 94 μF capacitor bank, which is comprised of eight 45 μF 6300 V capacitors (two series sets of four in parallel). Once charged to the required voltage level, the IGBT is pulsed on. This causes the current through the air-cored 75 mH inductor to ramp up at a constant di/dt, and, once the required peak inductor current is reached, the IGBT is turned off, causing the current to freewheel through the diode and thus turning it on. After a short off period (short enough to prevent a significant decrease in the inductor current level), the IGBT is pulsed on for a second time, and, due to the removal of stored charge in the device, a reverse recovery current flows through the diode until it can support the reverse voltage.

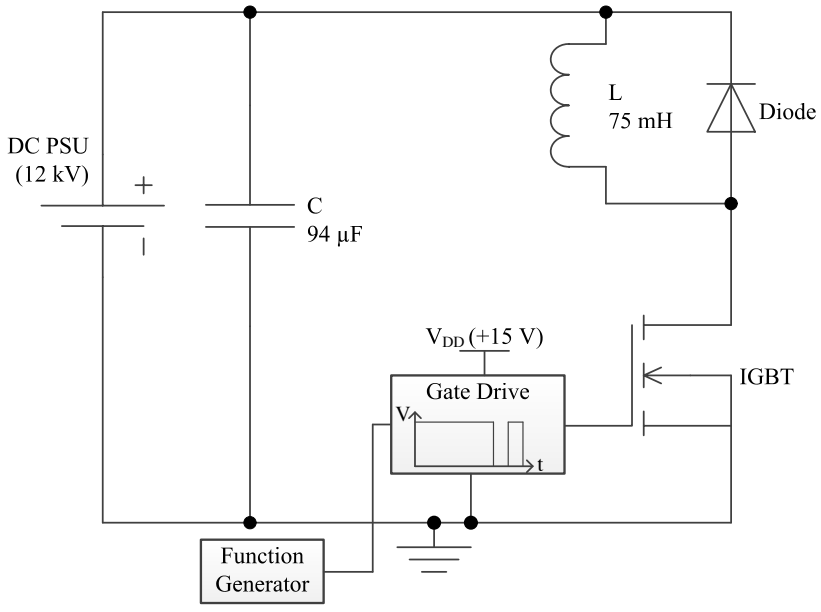


Figure 5.2: Schematic diagram of the chopper cell circuit used in the clamped inductive switching test rig. In this work, the diode is the device under test.

Figure 5.3: Clamped inductive switching test rig.

Due to the high voltage levels used for these tests, it has been necessary to submerge the semiconductor device dies in an insulating fluid (PMX-561 by Dow Corning) to prevent arcing and subsequent breakdown. This arrangement also facilitates both the cooling and heating of the device under test, so that the inductive switching performance can be evaluated over the temperature range -50°C to +250°C. Cooling to -50°C is achieved using a Tenney environmental chamber, whilst heating to +250°C is achieved by using a ceramic hotplate. In both cases, the temperature of the insulating fluid is measured by a

Type K thermocouple.

With regard to instrumentation of the inductive switching test rig, high-voltage, high-bandwidth probes (the PVM-12 by North Star Inc.) have been used to measure the diode voltage V_{AK} and the IGBT collector-emitter voltage V_{CE}. The diode current I_A has been measured using a Pearson Electronics current monitor (model 6656), and the IGBT gate-emitter voltage V_{GE} has been measured using a standard Tektronix oscilloscope probe. These circuit node voltages and currents have all been monitored on a Tektronix TDS5054B 4-channel digital oscilloscope. In order to drive the gate of the IGBT, a Tektronix AFG3022C function generator has been used to drive a HCPL-3020 optocoupler, which in turn drives the gate of the IGBT.

5.1.3.1 Carrier Lifetime Extraction Method

Though there are several electrical techniques that can be applied to extract the carrier lifetime of PiN diodes [142], an efficient method that can be employed is to calculate the carrier lifetime from the reverse recovery characteristics of the diode [143]. Using this method, the high-level carrier lifetime in the PiN diode can be expressed as

$$\tau_{HL} = 2 \cdot t_{rr} \frac{I_{RP}}{I_F} \tag{5.1}$$

where t_{rr} is the reverse recovery time, I_{RP} is the peak reverse current and I_F is the diode forward current. These parameters were shown diagrammatically in Chapter 3 (Figure 3.6). However, it is noted that the reverse recovery characteristics of PiN diodes depend not only on the effective carrier lifetime in the drift region, but also on the interface or surface generation. For mesa-isolated devices such as the ones fabricated in this thesis, it was reported in [144] that the reverse recovery characteristics are affected by recombi-

nation along the perimeter of the mesa. As such, it is possible to estimate the effective carrier lifetime excluding the mesa perimeter recombination component by examining the relationship between the high-level carrier lifetime determined from Equation 5.1 and the perimeter/area ratio of the PiN diode [143]. Due to the mesa perimeter recombination, the high-level carrier lifetime can also be defined by

$$\frac{1}{\tau_{HL}} = \frac{1}{\tau_{HL0}} + s_P \frac{P}{A} \tag{5.2}$$

where τ_{HL0} represents the effective high-level carrier lifetime due to the bulk properties as well as surface recombination, s_P is the surface recombination velocity along the mesa perimeter of the PiN diode, and A and P are the area and perimeter of the PiN diode mesa respectively. However, as outlined in [145], the surface recombination velocity of 4H-SiC is dependent on the surface treatment used, as well as the type of oxidation process applied [146]; this needs to be taken into account when estimating the carrier lifetime of the device according to Equation 5.2.

5.1.4 Contact Resistance Measurements

As metal-semiconductor contacts are an integral part of the devices being fabricated in this work, the measurement of these contacts is necessary in order to determine whether or not the contacts have ohmic (linear) or rectifying (non-linear) I-V properties. The resistance of ohmic contacts is of particular interest. Though there are several techniques that have been applied for determining the electrical characteristics of metal-semiconductor contacts [142], a widely-used technique, and one that has been applied in this work, is the transfer length method (TLM). The test structure required for the TLM contact resistance measurement is illustrated in Figure 5.4. Using this method, the total resistance between

any two adjacent contacts is given by

$$R_T = \frac{R_{sh}d}{Z} + 2R_C \approx \frac{R_{sh}}{Z}(d + 2L_T) \tag{5.3}$$

where L_T is the transfer length, which is defined as the distance over which most of the current transfers from the semiconductor into the metal, or vice versa. Equation 5.3 assumes that the contact length L is $\geq 1.5L_T$, where

$$L_T = (\rho_C/R_{sh})^{0.5} \tag{5.4}$$

in which ρ_C is the specific contact resistance, and R_{sh} is the sheet resistance. In the TLM contact resistance measurement, the total resistance (R_T) is measured for various contact spacings (d_x), and plotted against d, as shown in Figure 5.5. From this plot, it is possible to extract the sheet resistance from the slope $\Delta(R_T)/\Delta(d) = R_{sh}/Z$, the contact resistance R_C from the intercept at $d = 0$, which is $R_T = 2R_C$, and, lastly, the specific contact resistance from extrapolating the plot to $R_T = 0$, which gives $-d = 2L_T$.

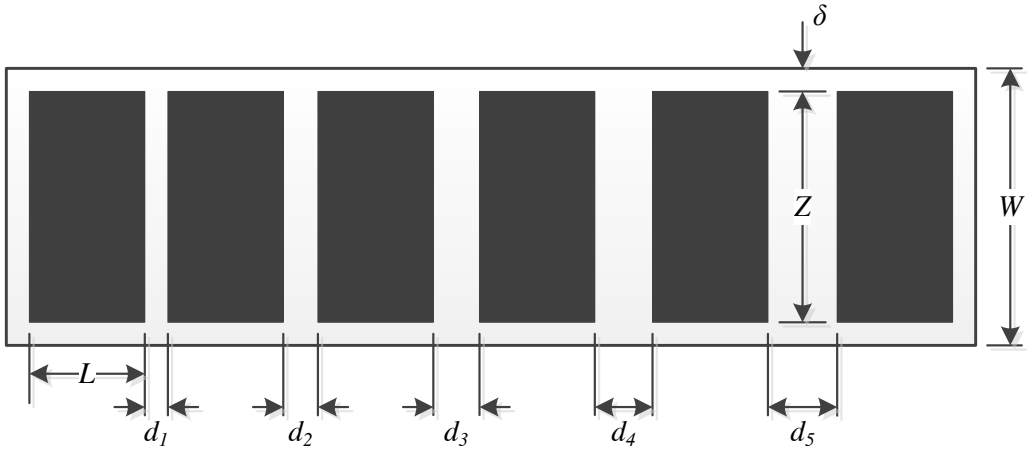


Figure 5.4: Transfer length method test structure.

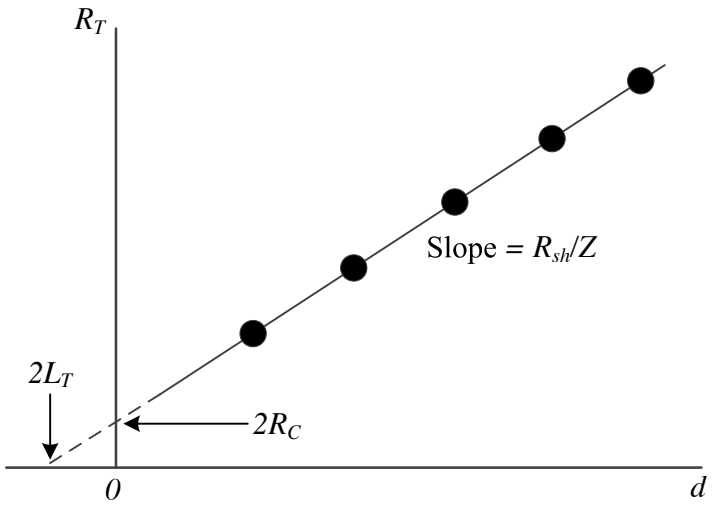


Figure 5.5: Transfer length method plot of total resistance as a function of contact spacing.

One principle disadvantage of the TLM contact measurement technique is that, after annealing, which is typically required for forming ohmic contacts to 4H-SiC, the sheet resistance underneath the contact pad will differ from that elsewhere in the semiconductor. As Equation 5.3 assumes that the sheet resistance is identical under the contacts and between the contacts, modified expressions for the front contact and the total resistance are required [147]:

$$R_{cf} = \frac{\rho_C}{L_{Tk}Z}\coth(L/L_{Tk}) \tag{5.5}$$

and

$$R_T = \frac{R_{sh}d}{Z} + 2R_C \approx \frac{R_{sh}d}{Z} + \frac{2R_{sk}L_{Tk}}{Z} = \frac{R_{sh}}{Z}\left[d + 2(R_{sk}/R_{sh})L_{Tk}\right] \tag{5.6}$$

where R_{sk} represents the sheet resistance underneath the contact and the transfer length is given by

$$L_{Tk} = (\rho_C/R_{sk})^{0.5} \tag{5.7}$$

It is still possible to extract R_{sh} and R_C from the R_T versus d plot; however, ρ_C cannot be determined as R_{sk} is unknown. In order to determine the value of R_{sk}, and thus ρ_C, additional experimental data, obtained from the "end resistance" measurement, is required. The end resistance measurement involves passing a current between two contact pads, and measuring the voltage between one of these contacts and an adjacent contact outside the current loop, as illustrated in Figure 5.6. The end resistance R_{ce} is simply V/I, and relating to the TLM parameters is found to be

$$R_{ce} = \frac{(R_{sk}\rho_C)^{0.5}}{Z\sinh(L/L_{Tk})} = \frac{\rho_C}{ZL_{Tk}\sinh(L/L_{Tk})} \tag{5.8}$$

Since

$$\frac{R_{ce}}{R_{cf}} = \frac{1}{\cosh(L/L_{Tk})} \tag{5.9}$$

and after eliminating R_{sk} in Equation 5.8, it is possible to determine L_{Tk} and thus ρ_C [147].

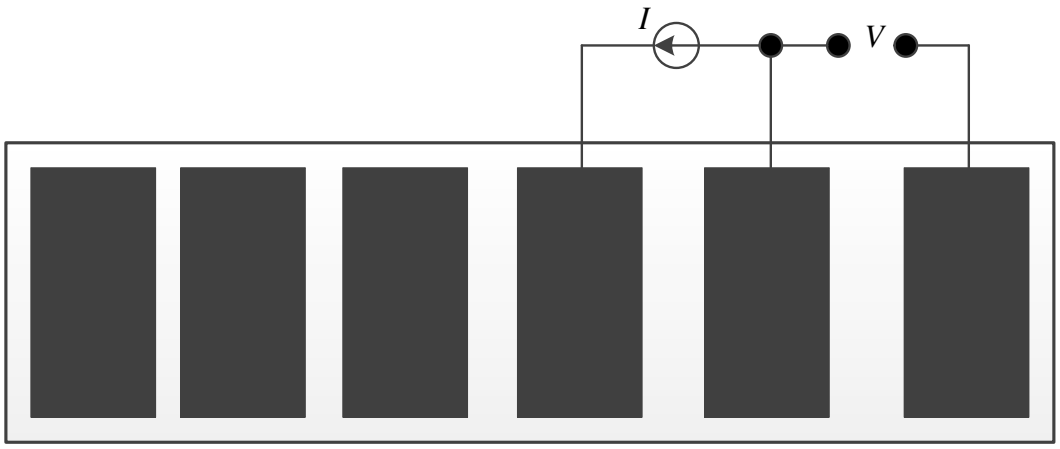


Figure 5.6: Transfer length method contact end resistance measurement topology.

In order to ensure that TLM contact resistance measurements are accurate, it is important that the electrical and geometrical contact parameters are constant across the

sample. Unfortunately, in practice, these parameters will typically vary across the sample, for example due to the presence of defects in the semiconductor. As such, the use of multiple test structures located across the sample is useful in reducing the measurement error. A second source of error in the measurement arises due to current flow and crowding in the gap region δ between the edge of the contact pads and the periphery of the mesa-etched TLM test structure, illustrated in Figure 5.4. As $\delta \neq 0$ in fabricated TLM test structures, it is found that incorrect intercepts of the R_T versus d plot can be problematic, leading to incorrect extracted values of contact resistance, transfer length and specific contact resistance. However, in the work by Chor and Lerdworatawee [148], it was found that for Z/δ ratios greater than 25, the errors arising due to the current flow and crowding in the gap region are negligible.

5.2 Physical Characterisation

In this Section, the physical characterisation methods that have been employed in the evaluation and analysis of the 4H-SiC PiN diodes fabricated in this work are discussed. Where the acronyms "SEM", "TEM" and "AFM" have been used, "M" is intended to mean either "microscopy" or "microscope".

5.2.1 Scanning Electron Microscopy

In order to evaluate the morphology of etched features in the 4H-SiC and SiO_2, scanning electron microscopy (SEM) has been employed. SEM is a reflection electron beam (e-beam) technique, using this e-beam to produce a magnified representation of the sample. When compared to optical microscopes, electron-based microscopes have the advantage of allowing much greater magnification, as electron wavelengths are much smaller than

photon wavelengths, and the depth of field is much higher. The electron wavelength λ_e is dependent on the electron velocity v or the accelerating voltage V, such that

$$\lambda_e = \frac{h}{mv} = \frac{h}{\sqrt{2qmV}} \tag{5.10}$$

where h is Planck's constant, q is the electronic charge and m is the mass of an electron. Assuming an accelerating voltage of 10 kV, the electron wavelength is 0.012 nm, much shorter than photon wavelengths of 400 to 700 nm, illustrating the advantages of electron microscopy over optical microscopy for high magnification imaging. A schematic representation of a scanning electron microscope is given in Figure 5.7. In this work, the Zeiss Supra 55-VP FEG-SEM located in the Physics Department at the University of Warwick has been used.

To obtain an SEM image, the electron gun emits a beam of incident electrons, which are focussed by the condenser lenses in the column of the instrument and scanned across the sample, with the secondary and/or backscattered electrons being detected to yield an image. Ideally, the electron beam should be bright and have a small energy spread. Of the different types of electron gun that are used in SEM, the field-emission gun (FEG) offers superior brightness and energy spread, as well as a longer working life. For most types of sample, incident electron energies typically range between 10-30 keV depending on the magnification factor being used, though for insulating samples lower electron energies, of the order of several hundred eV, are used to minimise sample charging. So that electrons can travel freely within the SEM, high vacuum levels are required, typically in the range 10^5 to 10^7 mbar.

A conventional SEM image is formed by detecting secondary electrons, which are ejected from the K-shell of atoms within the sample by inelastic scattering interactions

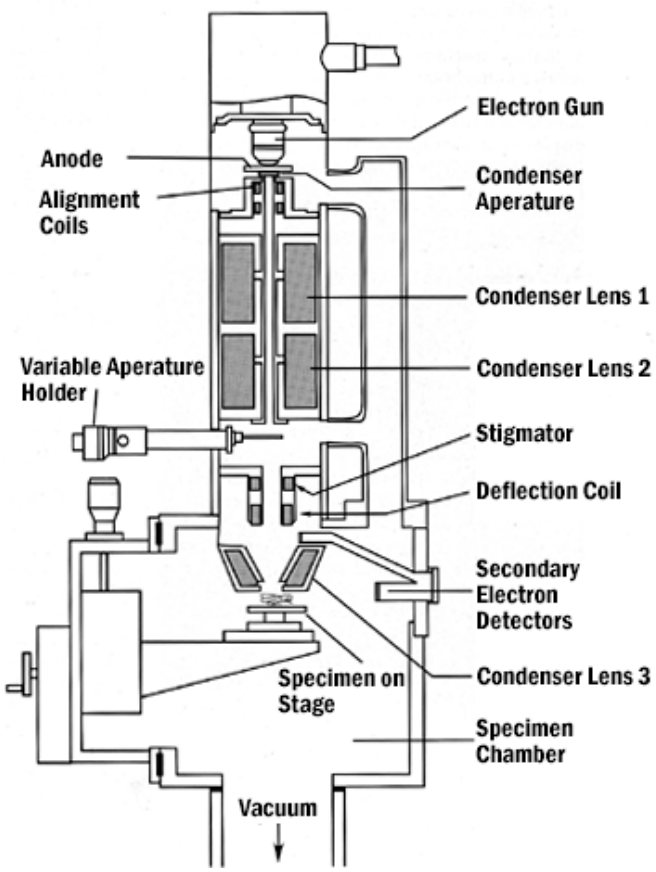


Figure 5.7: Schematic of a scanning electron microscope [149].

with the incident electrons. These secondary electrons are detected using an Everhart-Thornley (ET) detector, which is comprised of a scintillation material that emits light when struck by accelerated secondary electrons. This emitted light is channeled through a light pipe to a photomultiplier located outside of the SEM column, where the light incident on a photocathode generates electrons that are multiplied and used to drive the cathode ray display tube (CRT). By synchronising the CRT scan to the incident electron beam scan, the morphology of the sample can be visualised. It is also possible to store and view the SEM image digitally; in this case, the electrons generated by the photocathode will be subjected to analogue-to-digital conversion rather than being used to drive a CRT. The

magnification of the SEM image is dictated by the ratio of the CRT (or digital image) length to the sample scan length; magnifications in excess of 100,000× are possible in SEMs, though low magnifications are more difficult.

Although FEG-SEM instruments have an electron beam diameter of approximately 0.1 nm, the resolution that can be achieved in practice is typically worse than this, due to interactions of the incident electrons with the sample and the subsequent scattering of these electrons [142]. Another issue that can occur when using SEM for inspecting semiconducting samples is that of surface charging, which results in poor quality images. This can be eliminated by coating the surface with a thin conductive layer such as gold (Au), or by using a lower energy electron beam.

5.2.2 Transmission Electron Microscopy

Transmission electron microscopy, or TEM, has been applied in this work for high resolution imaging of metal-semiconductor structures, using the Jeol 2000FX TEM located in the Physics Department at the University of Warwick. The TEM is similar in principle to an optical microscope, in that it utilises a series of lenses to magnify the sample. As with the SEM, the TEM uses an election gun to generate a beam of electrons that are focussed on the sample by condenser lenses. However, unlike for the SEM, the sample in the TEM must be sufficiently thin, typically a few tens to a few hundred nm, to be transparent to electrons. This bypasses the resolution limitations caused by beam spreading encountered in SEM, and means that extremely high resolution, approaching 0.08 nm, can be achieved. However, a shortcoming of TEM is that it has limited depth resolution. Moreover, due to the requirement of very thin samples for TEM analysis, the sample preparation is considerably time consuming and requires specialist equipment. This especially applies to

4H-SiC, due to the hardness and chemical inertness of the material.

5.2.3 Atomic Force Microscopy

Atomic force microscopy (AFM) is a physical characterisation technique that allows the surface morphology of samples to be measured with atomic resolution in the z-axis, combining the features of a stylus profilometer with surface force apparatus. The basic components of an AFM are illustrated in Figure 5.8. For the work in this thesis, the Asylum Research MFP-3D AFM, located in the Physics Department at the University of Warwick, has been used.

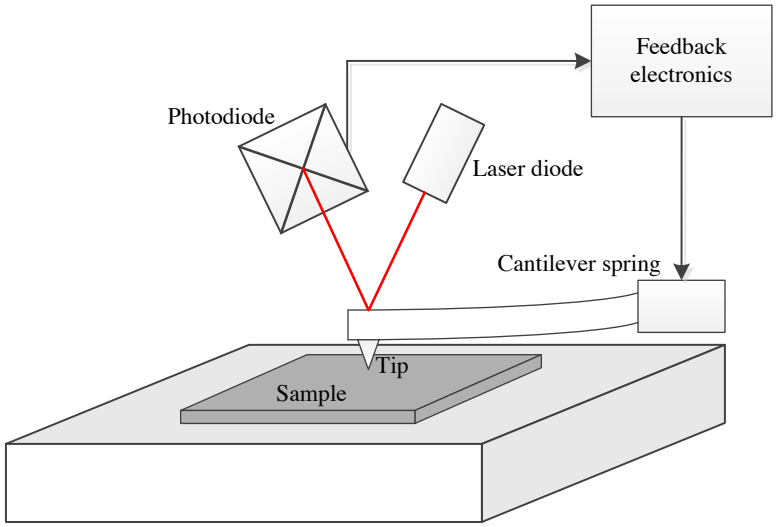


Figure 5.8: Schematic of an atomic force microscope.

An AFM image is obtained by scanning the cantilever tip over the surface of the sample, with the x- and y-axis scanning controlled using piezoelectric blocks. When the cantilever tip is brought into close proximity with the surface of the sample, forces between the tip and the sample result in a deflection of the cantilever, in accordance with Hooke's

law. This deflection is measured using a laser beam, which is reflected off the top of the cantilever into an array of photodiodes, with any change in displacement of the cantilever resulting in a change of output signal from the photodiode array. This signal is passed to the feedback electronics, which controls the cantilever.

There are several different methods for controlling the cantilever, though all AFM imaging performed in this work has been done using AC (or tapping) mode. This mode of operation involves driving the cantilever to oscillate up and down near its resonant frequency, and, due to the interaction of forces acting on the cantilever when the tip approaches the sample surface, the oscillation amplitude decreases with a decrease in distance between the tip and the sample. The height of the cantilever above the sample is controlled using a piezoelectric actuator, with the feedback electronics responsible for adjusting the cantilever height in order to maintain a set oscillation amplitude during the AFM scan. Using AC mode for AFM imaging is advantageous in that it circumvents the problem of the cantilever tip sticking to the sample surface, which can be problematic for non-contact AFM imaging when performed under normal ambient conditions. Furthermore, using AC mode minimises the damage done to the sample surface and the cantilever tip during AFM imaging.

5.2.4 X-Ray Diffraction

X-ray diffraction (XRD) is a physical characterisation technique that enables the identification of crystalline compounds, and has been used in this work to verify the presence of silicides and carbides, such as Ti_3SiC_2 and $NiSi_x$, at the metal-semiconductor interface of ohmic contact samples before and after annealing. The Panalytical X'Pert Pro MRD system located in the Physics department at the University of Warwick has been used for

all XRD work presented in this thesis. This XRD system is specifically designed for the analysis of thin films and single-crystal materials, and has the ability to orient the substrate at angles up to 8°, which is necessary for the 4H-SiC epitaxial substrates (which are oriented at 4° off-axis) studied in this work. For the XRD analysis of metal-semiconductor samples, coupled Omega-2Theta scans have been used, typically in the range 10-80°2θ.

The operation of the XRD system is based on Bragg's law, outlined by Sir William Henry Bragg and his son William Lawrence Bragg and subsequently published in the Cambridge Philosophical Society in 1914 [150]. Whilst attempting to provide an explanation as to how crystalline solids reflected x-rays at specific angles of incidence (θ), the theory of Bragg diffraction, or XRD, was proposed. This theory is illustrated in Figure 5.9. It is evident from this Figure that an x-ray beam incident on the crystalline solid is reflected off two separate planes of atoms, separated by a distance d. The beam that penetrates the first plane of atoms has to travel the additional distance shown as

$$AB + BD = 2AB \tag{5.11}$$

The geometry of the crystalline solid means that

$$AB = d\sin\theta \tag{5.12}$$

As such, the total additional distance that the x-ray beam has travelled is given by

$$2AB = 2d\sin\theta \tag{5.13}$$

In order for a signal to be detected, it is necessary that the two x-ray beams are in phase when they are summed, such that the reflections off the two planes of electrons interfere

constructively. Because constructive interference only occurs when the phase shift of the two x-ray beams is 2π, the condition required for a signal to be detected can be expressed as

$$n\lambda = 2d\sin\theta \tag{5.14}$$

where n is an integer and λ is the wavelength of the x-ray beams. This expression is referred to as Bragg's law. By scanning a crystalline solid by 2θ, a set of peaks corresponding to the d spacings of the crystalline material being examined can be revealed. Each material has a unique set of d spacings, therefore it is possible to identify a particular material from comparison and matching from a database.

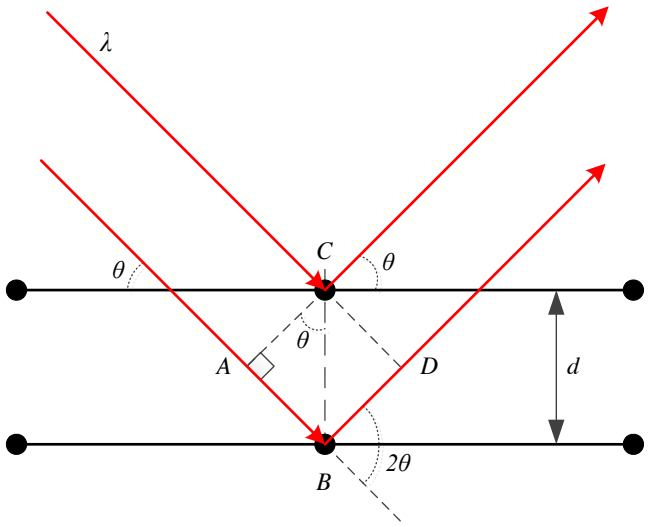


Figure 5.9: Diagram illustrating the geometry of crystalline solids associated with Bragg's Law.

5.2.5 Secondary Ion Mass Spectrometry

In work in this thesis, secondary ion mass spectrometry (SIMS) has been applied to determine the distribution of implanted dopant species in the 4H-SiC semiconductor material. In SIMS, the surface of the semiconductor is bombarded with a focussed ion beam, resulting in the semiconductor material being sputtered and partly ionised. This ionised component is then analysed in a mass spectrometer. All SIMS work presented in this thesis has been carried out at Loughborough Surface Analysis, Ltd [151].

There are two main variants of SIMS, the static SIMS technique, and the dynamic SIMS technique. Static SIMS involves the use of an ion beam with very low current density, resulting in only a small amount (<1%) of the original surface of the sample being consumed during the analysis. The material that is sputtered from the surface of the sample is predominantly in the form of molecular fragments, which reflect the sample's surface chemistry. As such, by analysing the patterns of these molecular fragments, it is possible to identify any surface contaminants.

The dynamic SIMS technique, which is the technique relevant to the work in this thesis, involves the use of an ion beam with a much higher current density. During the course of the analysis, the sample surface is continuously sputtered, and, by monitoring the signals from the elements that are of interest (in this case the implanted dopant species) as a function of time, a depth profile of these elements is produced. A schematic of a typical dynamic SIMS instrument is shown in Figure 5.10. The ion beam is generated by the primary ion gun, of which there are three different types that can be employed, depending on the analysis requirements. For the dynamic SIMS technique that requires a high current density ion beam, oxygen or caesium primary ions are typically used, depending on whether the elements being investigated are electropositive or electronegative.

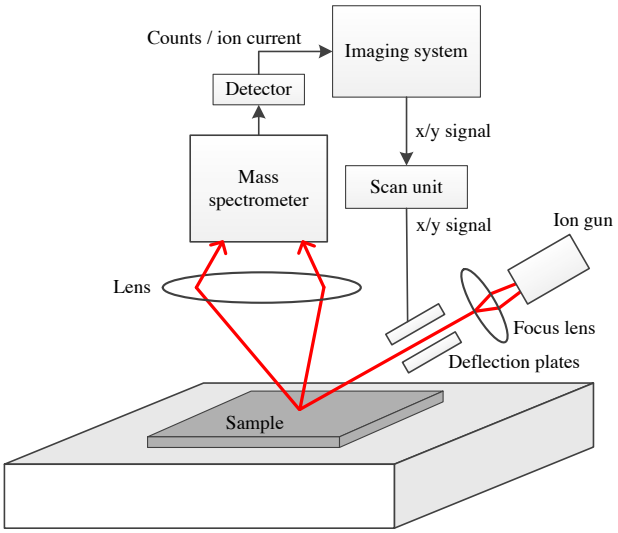


Figure 5.10: Schematic of a typical dynamic SIMS instrument.

Once the primary ion beam ionises and sputters some of the atoms off the surface of the sample, the secondary ions are collected by ion lenses and filtered according to their atomic mass in the mass spectrometer. Again, depending on the type of SIMS technique that is being used, there are three different mass analysers that can be employed: the sector field mass spectrometer, the quadrupole mass spectrometer, and the time-of-flight mass spectrometer. The SIMS equipment used in this work employs sector field mass spectrometry, which separates the secondary ions according to their mass to charge ratio using a combination of an electrostatic analyser and a magnetic analyser. Finally, the secondary ions are detected by means of a Faraday cup, which measures the ion current and outputs it to the imaging system. By deflecting the primary ion beam in the x-y axis on the sample, it is possible to obtain a 3-D map of the element distribution within the sample.

Because it is based on mass spectroscopy, SIMS is capable of detecting any known element with a sensitivity in the ppm to ppb range. However, due to the sputtering

of the sample surface during the analysis, some 'cratering', of the surface, the size of which is dependent on the primary ion beam diameter, is unavoidable. Finally, it is important to note that SIMS is only capable of determining the total implanted dopant atom concentration, and not the electrically-active dopant concentration.

5.2.6 Raman Spectroscopy

Raman spectroscopy is a technique based on the inelastic scattering of monochromatic light, first demonstrated in 1928 by Sir C. V. Raman, whom the technique has since been named after. In this work, Raman spectroscopy has been applied to determine the effectiveness of annealing processes used to recover crystal damage inflicted during ion implantation as well as the free carrier concentration in the implanted regions of the devices. All Raman spectroscopy performed in this thesis has been carried out using a 244 nm DUV laser within the Department of Physics at the University of Bath, UK [152].

In Raman spectroscopy, light from a laser source interacts with molecular vibrations, phonons or other excitations in the system, which results in the energy of laser photons being shifted up or down. This shift in energy is utilised to give information concerning the vibrational modes in the system. An energy level diagram showing the states involved in a Raman signal is shown in Figure 5.11. Due to it having relatively low absorption coefficients in the visible region, thus giving large penetration depths for Raman probe lasers, the analysis of ion implanted regions in SiC typically requires a UV laser. For a laser wavelength of 244 nm, a penetration depth of 50-100 nm is expected [153]. A detailed discussion of the theory of Raman spectroscopy is given in [154].

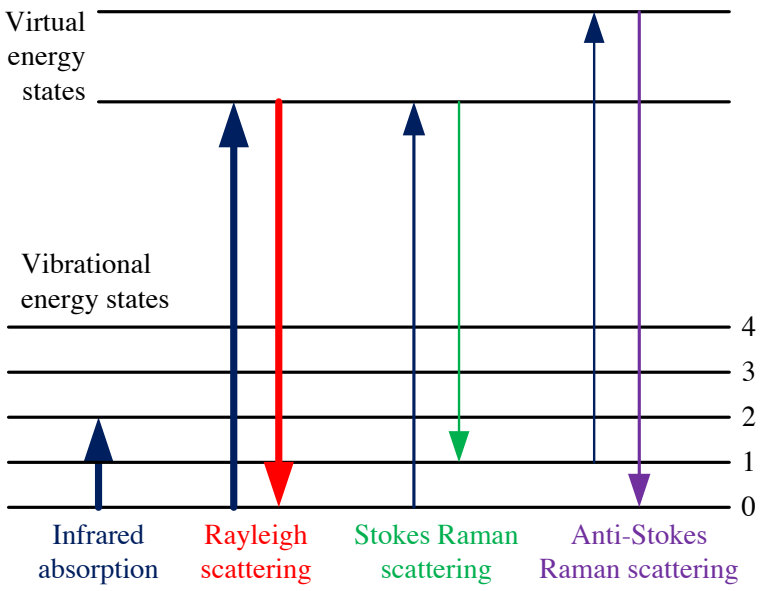


Figure 5.11: Energy level diagram showing the states involved in a Raman signal. The line thicknesses are approximately proportional to the signal strength from the different transitions.

5.3 Summary

In this Chapter, both the electrical and physical characterisation techniques that will be applied to the 4H-SiC power devices fabricated in this thesis have been presented. Details of the characterisation equipment, both electrical and physical, that will be used have been provided, in addition to the specific techniques that will be used to extract important device parameters such as ohmic contact resistance and carrier lifetime.

Chapter

6 Fabrication Process Development for 4H-SiC PiN Diodes

In this Chapter, the fabrication processes required for high voltage 4H-SiC PiN diodes that have been developed are presented. Firstly, characterisation and optimisation of dry etching processes was carried out. Following this, a study into the formation of low-resistance, reliable ohmic contacts to p-type 4H-SiC has been undertaken, encapsulating both electrical and physical characterisation to determine the mechanisms behind the performance of these contacts.

6.1 RIE and ICP Etching Characterisation

The etching of 4H-SiC typically demands the use of RIE or ICP etch methods, due to the high temperatures required for wet etching processes, as described in Chapter 3. For the high voltage devices fabricated in this work, the profile of the etched 4H-SiC mesa sidewalls is important, as rough, jagged features can enhance electric field crowding and thus reduce the breakdown voltage capability of the device [76]. Moreover, poor surface morphology resulting from etching processes can increase the surface recombination rate

due to defect centres created, thus reducing the overall carrier lifetime in the device. As such, the use of an optimised 4H-SiC etch method is crucial if high performance PiN diodes are to be realised.

As well as the etching of 4H-SiC, the etching of the mask used for the 4H-SiC etch is also important, as it is the profile of this that dictates the profile of the etched 4H-SiC features. Masking materials that have been deployed in this work include photoresist, SiO_2 and NiV. However, in order to prevent micro-masking, the deposition of NiV masking layers directly onto the 4H-SiC material has been avoided [76]. The etch rates and mask selectivity of etch processes that have been experimentally determined in this work are summarised in Table 6.1. In order to measure etch steps heights, an Ambios Technology stylus profileometer has been used. One fundamental observation that can be made from the data in Table 6.1 is the vast difference in etch rate between the RIE and ICP processes for the SiO_2 etch, which, coupled with the fact that RIE processes typically inflict more damage on the etched surface, makes ICP etching the preferred technique to use. Though not shown in the Table, the RIE etch rate for 4H-SiC was markedly slower than the ICP etch rate, etching at a rate of approximately 12 nm/min, rendering it impractical for etching features greater than a few hundred nm in depth.

Initial characterisation of SiC etching involved using a tetraethyl orthosilicate (TEOS) SiO_2 mask, itself masked by S1818 photoresist to enable patterning of the SiO_2. After photolithography, the SiO_2 was patterned using the SiO_2 vertical ICP etch for a duration sufficient to penetrate the SiO_2 mask. However, due to inadequate heat sinking of the 4H-SiC sample during the etch, the photoresist was heat-damaged during this process. The photoresist was then removed in O_2 plasma, and the SiC was etched using the 50 SF_6 + 3 O_2 1000 W ICP program. Upon completion of the SiC etch, the remaining SiO_2 mask was removed in HF solution. SEM was then used to observe the profile of the

etched SiO_2 and SiC. Figure 6.1 illustrates the profile of etched SiO_2 mesa mask after the photoresist was removed. It is evident from this Figure that not only are the sidewalls of poor morphology due to the photoresist being heat-damaged, but the surface of the SiO_2 from which the photoresist has been removed also shows signs of damage. As shown in Figure 6.2, this poor morphology of the SiO_2 mask has been replicated when etching the 4H-SiC, which would clearly have implications for the electrical performance of the device.

Table 6.1: Summary of etch rates and mask selectivity for RIE/ICP etch processes.

Etch process	Mask used	Etch rate (nm/min)	Selectivity
SiO_2 RIE (100 CHF_3 + 5 O_2, 170 W)	Photoresist	∼28	1.5
4H-SiC (50 SF_6 + 3 O_2, 1000 W ICP)	SiO_2	∼820	1.7
4H-SiC (50 SF_6 + 3 O_2, 1000 W ICP)	NiV	∼735	20
SiO_2 vertical ICP etch (800 W ICP)	Photoresist	∼415	1.6
SiO_2 sloped ICP etch	Photoresist	∼535	2.0

In order to prevent this problem of poor morphology resulting from the use of a heat-damaged photoresist mask, it was clear that either the etching process had to be modified so that the photoresist would not become damaged, or, alternatively, the use of photoresist for masking the SiO_2 during the ICP etch had to be eliminated. Unfortunately, because of the design of the RIE/ICP etching equipment, it is difficult to achieve satisfactory heat sinking when using small (sub-4 inch) wafer samples, as these samples have to be mounted on a Si carrier wafer and thus do not gain the benefit of the helium chuck that thermally connects the 4 inch wafer to the chiller system. Another possible option could be to decrease the power of the ICP etching program and correspondingly increase the etch time, though due to the unsatisfactory heat sinking performance, this is still potentially problematic. It was therefore decided to eliminate the use of photoresist during any ICP etch programs, instead using a NiV mask. Though this adds additional processing steps,

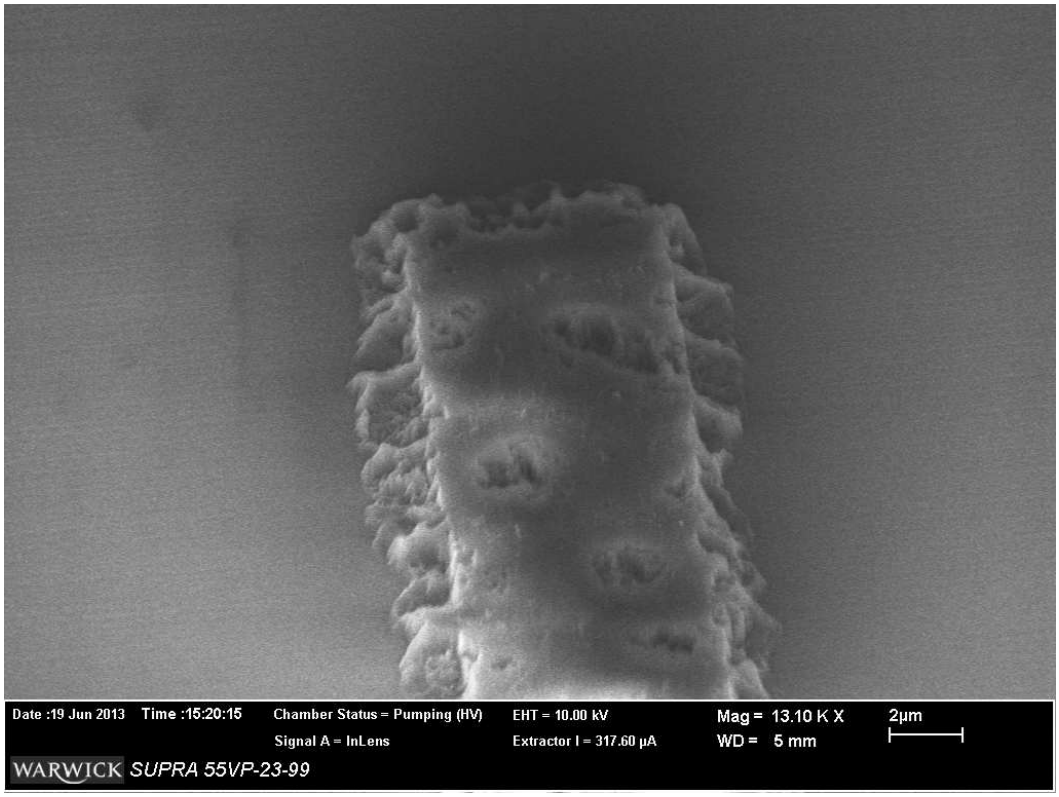


Figure 6.1: ICP etched SiO_2 mask patterned using photoresist (photoresist mask removed prior to SEM imaging).

the NiV is a lot less susceptible to the heat generated during ICP etching than photoresist, and should result in better 4H-SiC feature definition. Figures 6.3 and 6.4 show the profile of an etched 4H-SiC mesa sidewall after mask removal; it is evident that the surface quality is significantly improved. In addition, the masked surface of the 4H-SiC was unaffected by the etch process, as intended. The sidewalls now exhibit a smooth texture, though the shortcomings of the photolithography, which have resulted in striation of the sidewalls, are visible [155]. Due to the relatively large size of the devices fabricated in this work compared to the sidewall imperfection this is not considered to be a cause for concern; however, it is noted that further refinement of photolithographic feature definition would be required for devices that rely on a uniform sidewall, such as trench MOSFETs.

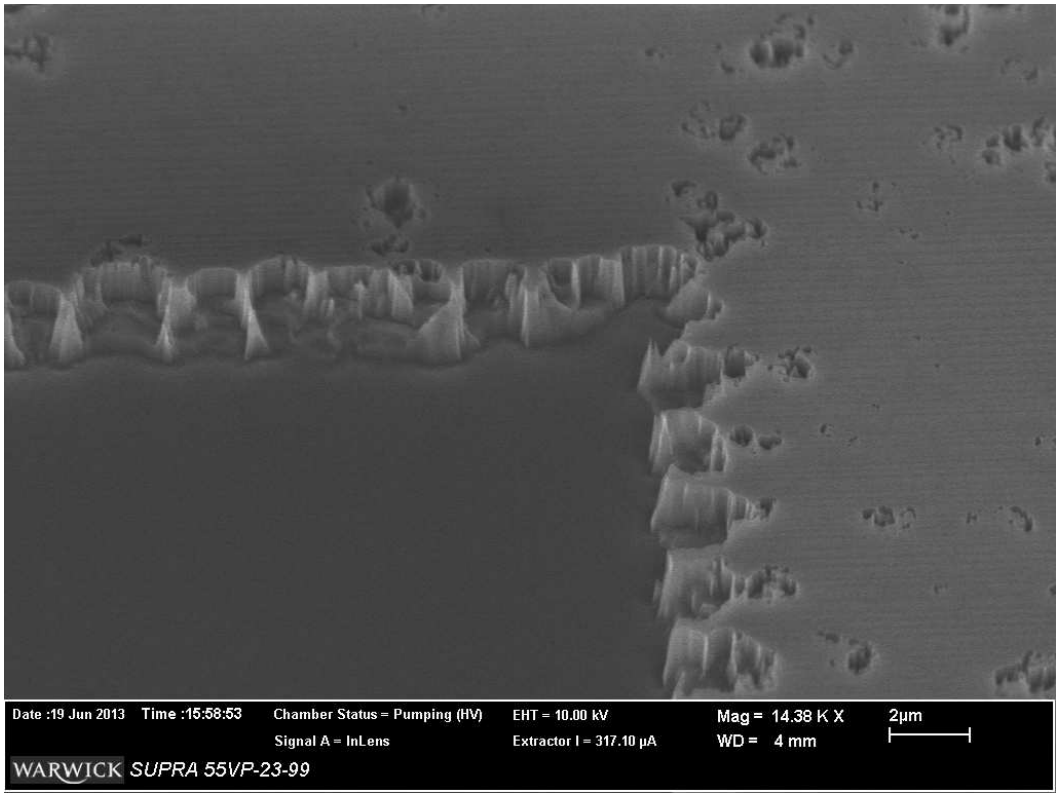


Figure 6.2: ICP etched SiC mesa sidewall with SiO_2 mask patterned using photoresist (SiO_2 mask removed prior to SEM imaging).

6.2 P-type Ohmic Contact Study

As discussed in Chapter 3, the formation of good quality, low resistance ohmic contacts to p-type 4H-SiC continues to present a challenge for 4H-SiC semiconductor devices. As such, this process has been optimised to achieve low specific contact resistivity. In this thesis, metal deposition for ohmic contacts has been achieved using a sputtering system [156], and metal schemes have been limited to Al, NiV and Ti. Annealing of contacts has been performed using a rapid thermal anneal (RTA) furnace in an inert (Ar) atmosphere, and the electrical performance of these contacts has been measured using the TLM technique discussed in Chapter 5. The TLM structure dimensions are illustrated in Figure 6.5. The

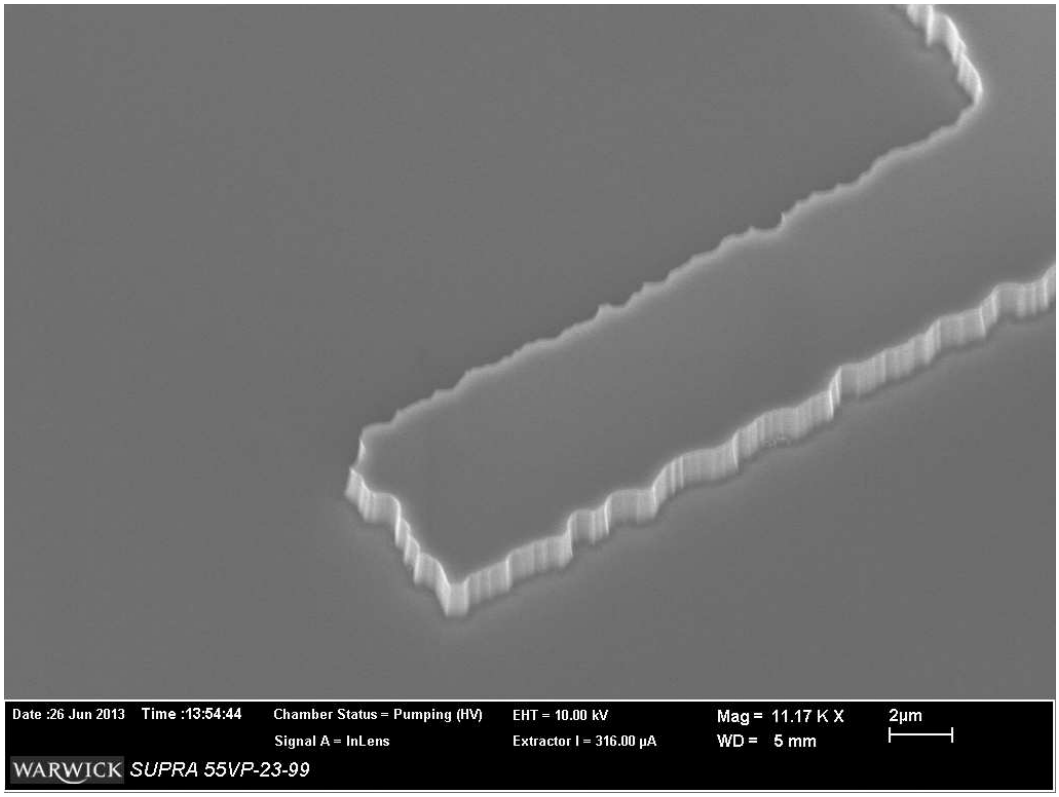


Figure 6.3: ICP etched SiC mesa sidewall with SiO_2 and NiV mask (1). Both SiO_2 and NiV mask layers were removed prior to SEM imaging.

4H-SiC substrate used for this study was sourced from Dow Corning, with the p-type epitaxial layer (0.25 μm doped at $>1\times10^{19}$ cm^{-3}) being grown at Norstel. This epitaxial substrate was laser-cut into 8×8 mm dies for subsequent processing.

6.2.1 Fabrication Process for TLM Structures

The first stage of processing the TLM structures is the cleaning of the 4H-SiC dies, as outlined in Appendix B. Following this, one micron of TEOS SiO_2 was deposited to serve as the TLM isolation etch mask. The TLM isolation features were defined using the photolithography process described in Appendix C. The TEOS SiO_2 was etched using

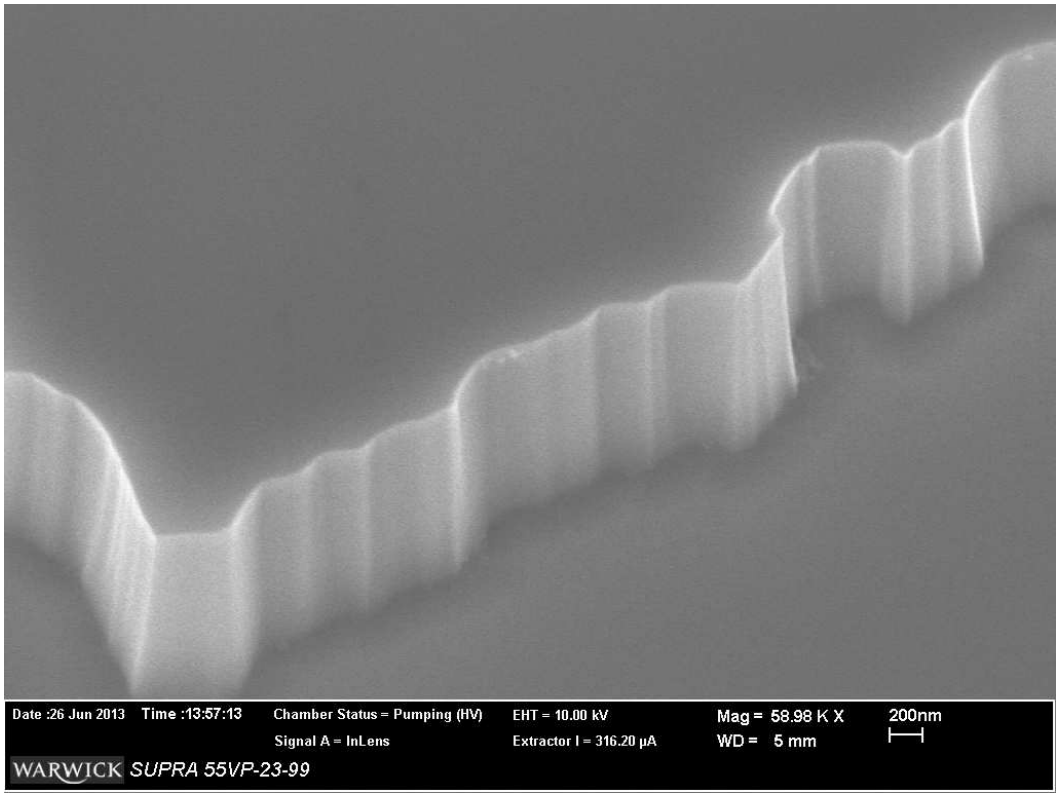


Figure 6.4: ICP etched SiC mesa sidewall with SiO_2 and NiV mask (2). Both SiO_2 and NiV mask layers were removed prior to SEM imaging.

RIE, to obtain a vertical sidewall whilst maintaining the photoresist morphology. After removal of the photoresist in an O_2 plasma, the exposed SiC was ICP etched to a depth of ∼500 nm.

Once the TLM isolation features had been defined and the TEOS SiO_2 mask removed in dilute HF solution, a second layer of TEOS SiO_2, again one micron thick, was deposited. After the photolithography process to define the TLM contact pad regions, the TEOS SiO_2 was etched to a depth of ∼800 nm using RIE. The remaining ∼200 nm of TEOS oxide was then etched away through to the SiC surface using 10:1 buffered oxide etch (BOE), and the samples were rinsed in DI water. This provides an undercut to the contact pad features, which facilitates easier lift-off during the subsequent metallisation

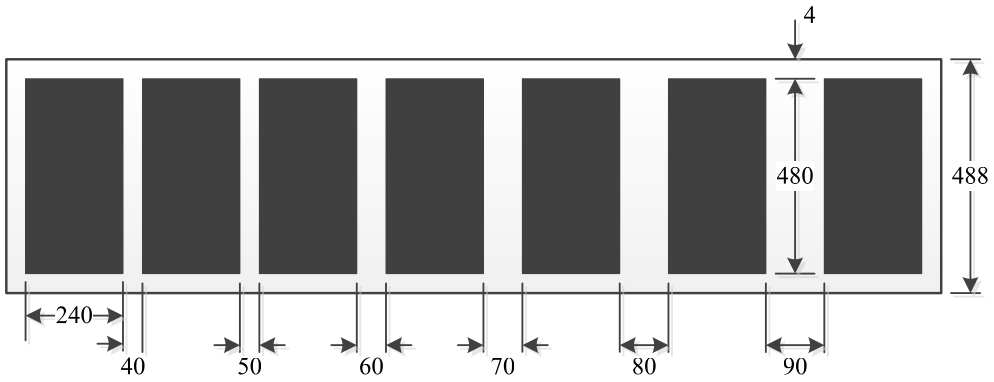


Figure 6.5: Fabricated TLM structures (all dimensions are in μm).

process. Following the BOE, the relevant metal scheme was deposited onto the die at a base pressure of $<1\times10^{-6}$ Torr, and the unwanted metal and photoresist removed in acetone using an ultrasonic bath. Finally, the metallised die was then annealed using the RTA furnace under the relevant annealing conditions.

6.2.2 Electrical Characterisation Results

To electrically characterise the metal-semiconductor contacts described in this Chapter, an Agilent Technologies B1500A Semiconductor Parameter Analyser in conjunction with four probes (two each for force and sense) has been used, with all measurements being taken under dark conditions. The first metal scheme that was investigated was an Al/Ti/Al stack, with corresponding thicknesses of 100/100/10 nm. This particular metal scheme yielded the lowest specific contact resistance (5×10^{-6} Ω-cm^2) in the work presented by Jennings et al. [3], surpassing the performance of a range of other Ti-, Al- and Ni-based metal schemes for p-type 4H-SiC.

The investigation into the Al/Ti/Al metal scheme involved performing anneals at both 1000°C and 1050°C, each for durations of 2 and 4 minutes. Prior to annealing, it

was confirmed that the contact structures had a rectifying I-V characteristic, as shown in Figure 6.6. However, as summarised in Table 6.2, ohmic behaviour was only achieved using an annealing temperature of 1000°C for a duration of 4 minutes. when comparing these results with the results presented in [3], it is evident that the electrical characteristics of the Al/Ti/Al contacts fabricated in this work are markedly inferior. On visual inspection of the as-deposited metallised samples that were predominantly Al-based, the Al appeared to be dull and white in colour, as opposed to being shiny and silver, which was expected. This suggested that the Al had oxidised to some extent after (or during) the sputtering deposition, therefore degrading the ohmic properties of the metal contact. As such, further ohmic contact investigation focussed on metal schemes with a reduced Al concentration, and with Ti used as the initial metal layer.

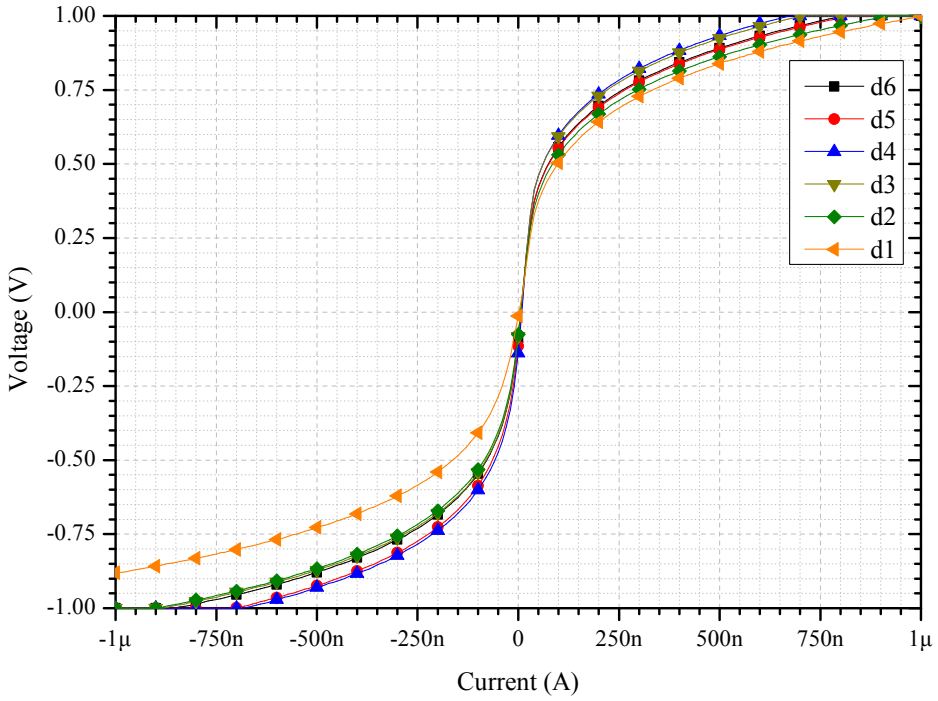


Figure 6.6: Rectifying I-V characteristics of unannealed Al/Ti/Al ohmic contact scheme (d_1 to d_6 refer to contact spacings). Measurements were taken at 25°C.

Table 6.2: Summary of electrical characterisation results for Al/Ti/Al p-type contact structures.

Sample ref.	Anneal temp. (°C)	Duration (minutes)	Contact res. (Ω-cm^2)
Al/Ti/Al_1	1000	2	Rectifying
Al/Ti/Al_2	1050	2	Rectifying
Al/Ti/Al_3	1000	4	2.8×10^{-4}

The next metal scheme that was investigated for use as a p-type ohmic contact was Ti/Al/NiV, with corresponding thicknesses 30/90/25 nm. The use of Ti/Al-based metal contacts to p-type 4H-SiC has been widely found to yield low contact resistances, as summarised in [121]. Moreover, it has been reported that in Ti/Al-based contact structures, metallic compounds are formed during the annealing process, which serve to lower the height of the inherent Schottky barrier that is present and promote current flow through the contact structure [120]. A thin NiV top layer was used, the intention of which was to prevent the Al from oxidising, as was observed in the previous contact structures that were fabricated.

The results for the Ti/Al/NiV ohmic contact structures for a range of annealing temperatures are shown in Figure 6.7. As with the Al/Ti/Al metal scheme, it was found that non-annealed samples had rectifying characteristics. It can be seen that the specific contact resistivity is strongly dependent on annealing temperature; performing the anneal at 1000°C with a 2 minute pre-anneal at 600°C yielded the lowest specific contact resistance values. Further annealing experiments were performed using this 600+1000°C process, for a range of hold times at 1000°C; these results are shown in Figure 6.8. It was found that an anneal time of 2 minutes was the optimum duration; longer anneal times resulted in ohmic contacts with higher specific contact resistance values.

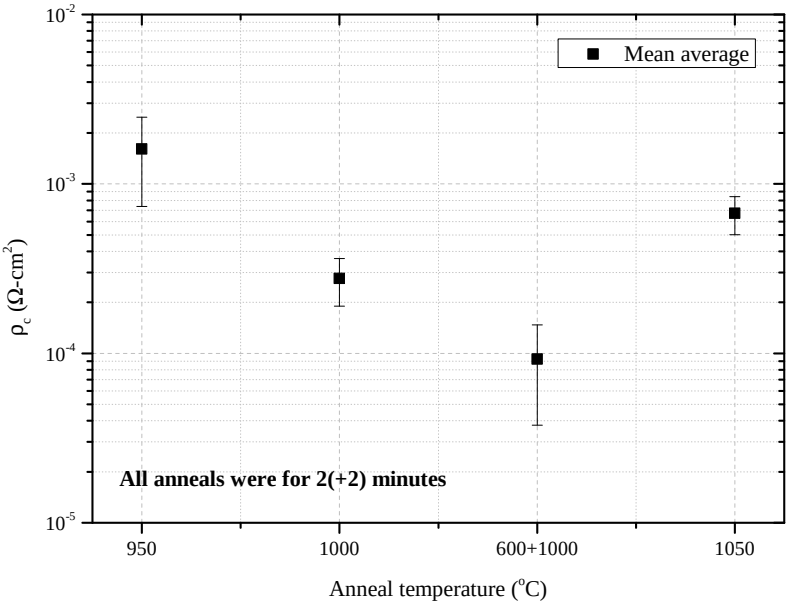


Figure 6.7: Specific contact resistance of Ti/Al/NiV ohmic contacts as a function of annealing temperature.

Though the Ti/Al/NiV metal scheme has yielded low specific contact resistivity values to p-type 4H-SiC, it was observed during the fabrication of TLM structures that the lift-off process occasionally caused some of the NiV layer to peel away from the rest of the sample, suggesting poor adhesion to the underlying layer. As such, it was decided to remove the NiV top layer and investigate the use of a Ti/Al metal scheme, with corresponding thicknesses of 30/90 nm (identical to the Ti/Al layers in the Ti/Al/NiV metal scheme). By using a 2 minute 1000°C anneal with a 2 minute 600°C pre-anneal, a mean specific contact resistance of 5.3×10^{-6} Ω-cm^2 was achieved, which was significantly lower than other metal schemes investigated previously.

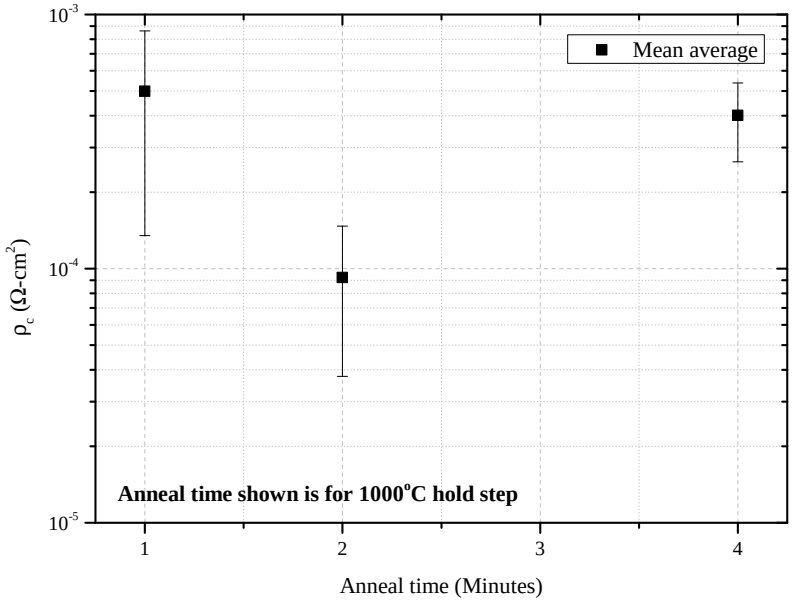


Figure 6.8: Specific contact resistance of Ti/Al/NiV ohmic contacts as a function of annealing time.

6.2.3 TEM / SEM Analysis

In order to gain an understanding of the physical structure of the metal-semiconductor interface both before and after annealing, TEM and SEM have been employed. Because the Ti/Al/NiV metal scheme has yielded low resistance ohmic contacts and consists of all three of the metals investigated in this study, the physical characteristics of this metal scheme were of particular interest.

Figure 6.9 shows a low resolution (LR) TEM image along the 11-20 zone axes of 4H-SiC of the Ti/Al/NiV metal scheme prior to annealing. It is evident from this Figure that there is an amorphous layer (light contrast) present in some areas of the Al/NiV interface, which is suspected to be due to oxidation during the metallisation process (this layer is more visible in Figure 6.13). This indicates that the vacuum system used during

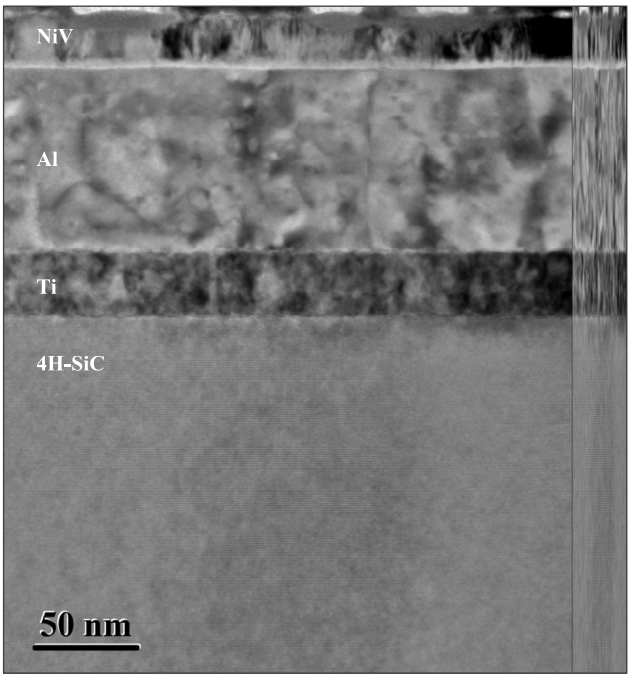


Figure 6.9: LR-TEM image of non-annealed Ti/Al/NiV metal scheme.

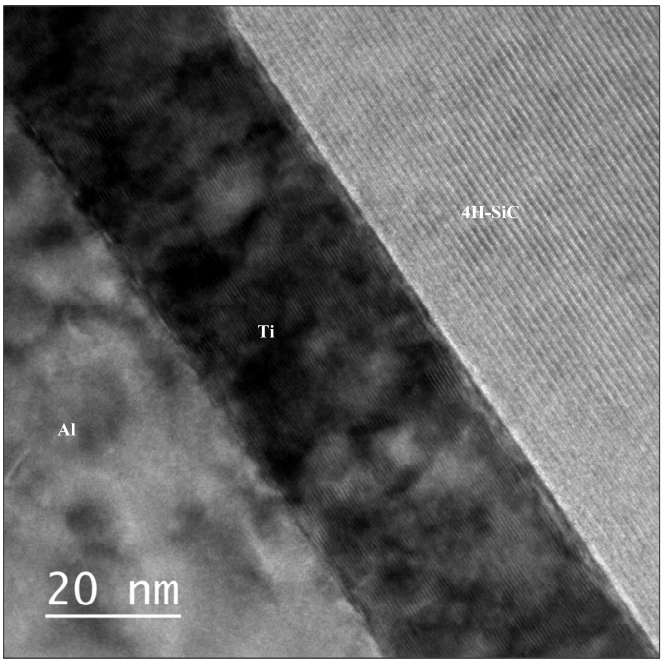


Figure 6.10: HR-TEM image showing the 4H-SiC/Ti and Ti/Al interfaces.

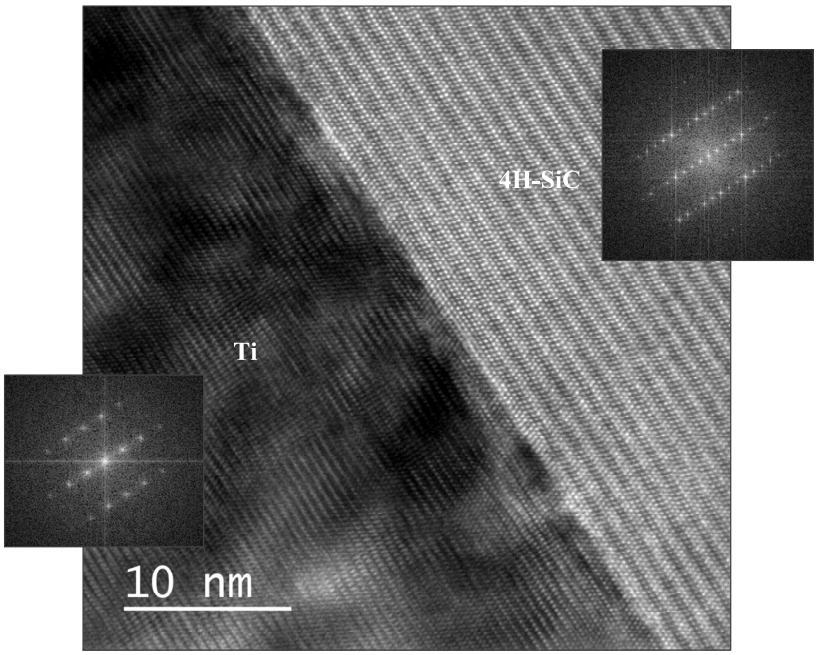


Figure 6.11: HR-TEM image of the 4H-SiC/Ti interface and the FFT of the crystal structures illustrating the epitaxial arrangement of Ti on 4H-SiC.

the metallisation is inadequate and detrimental to the quality of the metal contacts that can be achieved, and potentially explains the poor NiV adhesion that was observed as well as the improvement in electrical characteristics when not using the NiV top layer. To the right of the Figure, the image has been laterally compressed to highlight the interface roughness; it can be seen that the metal layers are uniform in nature.

Figure 6.10 shows a high resolution (HR) TEM image of the 4H-SiC/Ti and Ti/Al interfaces. It is evident that the Ti is deposited epitaxially onto the 4H-SiC; this is further illustrated in Figure 6.11, which shows a high resolution image of the 4H-SiC/Ti interface, along with the Fast Fourier Transform (FFT) showing the corresponding hexagonal crystal structure of the Ti and 4H-SiC. This epitaxial arrangement of the 4H-SiC/Ti can be attributed to the fact that the two materials have similar lattice constants; for 4H-SiC, a = 3.07 Å, whilst for Ti a = 2.95 Å. The Ti/Al interface is shown further in Figure

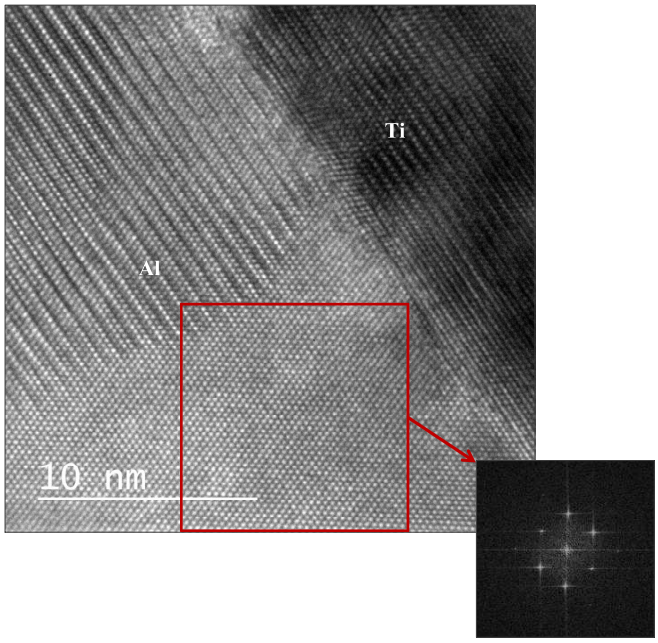


Figure 6.12: HR-TEM image of the Ti/Al interface and the FFT of the Al crystal structure.

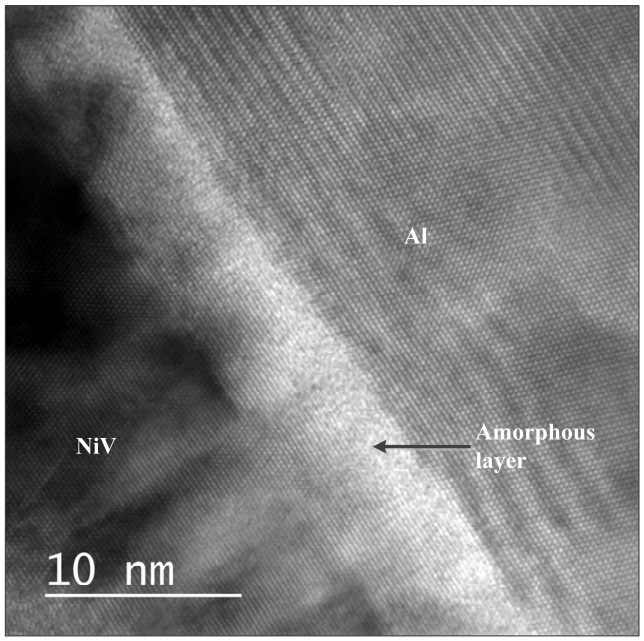


Figure 6.13: HR-TEM image of the Al/NiV interface.

6.12, where it can be seen that the Al has a polycrystalline structure. The FFT taken in the area of the image enclosed by the red square illustrates the face-centred cubic structure of the Al, which, in this area, grows along the <111> direction of top of the Ti. Finally, Figure 6.13 shows the Al/NiV interface, highlighting the presence of the ∼6 nm amorphous layer suspected to be SiO_2 (due to the non-optimal vacuum during the metal deposition process discussed previously). The NiV layer is of poorer structural quality that the Ti and Al metal layers, being predominantly amorphous.

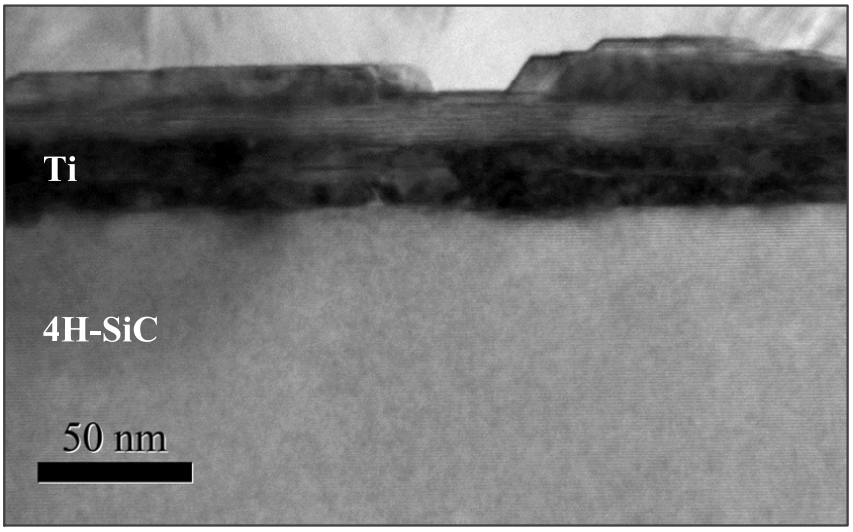


Figure 6.14: LR-TEM image of annealed Ti/Al/NiV ohmic contact.

Figures 6.14 and 6.15 show TEM images of the Ti/Al/NiV metal scheme after annealing at 1000°C for 2 minutes. It is evident that the annealing process has had a significant effect on the structure and composition of the metal scheme; the Al and NiV layers are no longer evident, and the remaining Ti-based alloy layer (confirmed by EDAX) is inhomogeneous, no longer displaying the uniform morphology that was observed in the non-annealed samples. However, because the anneal temperature is far in excess of the melting point of Al, a change in morphology of the metal scheme is expected. In order

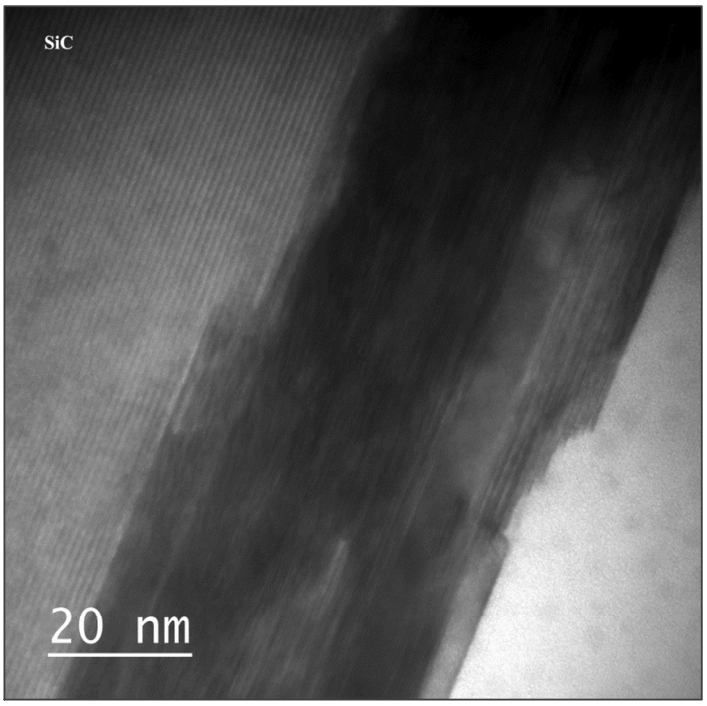


Figure 6.15: HR-TEM image of annealed Ti/Al/NiV ohmic contact. The region of dark contrast represents a Ti-based alloy, which was confirmed by EDAX.

to further characterise the morphology and composition of the annealed metal contact, SEM / EDAX has been employed. Figure 6.16 shows an SEM image of an area of the annealed Ti/Al/NiV ohmic contact; the varying morphology of the metal is evident here, and is quantified in the EDAX spectra shown within the Figure. It is evident that there different regions which are Ni-rich, Al-rich and also Si-rich; this suggests that the annealing process needs optimising if a homogeneous metal layer is to be achieved. However, due to the need to anneal at high temperature in order to form metallic phases at the metal-semiconductor interface, achieving a homogeneous layer may not be possible.

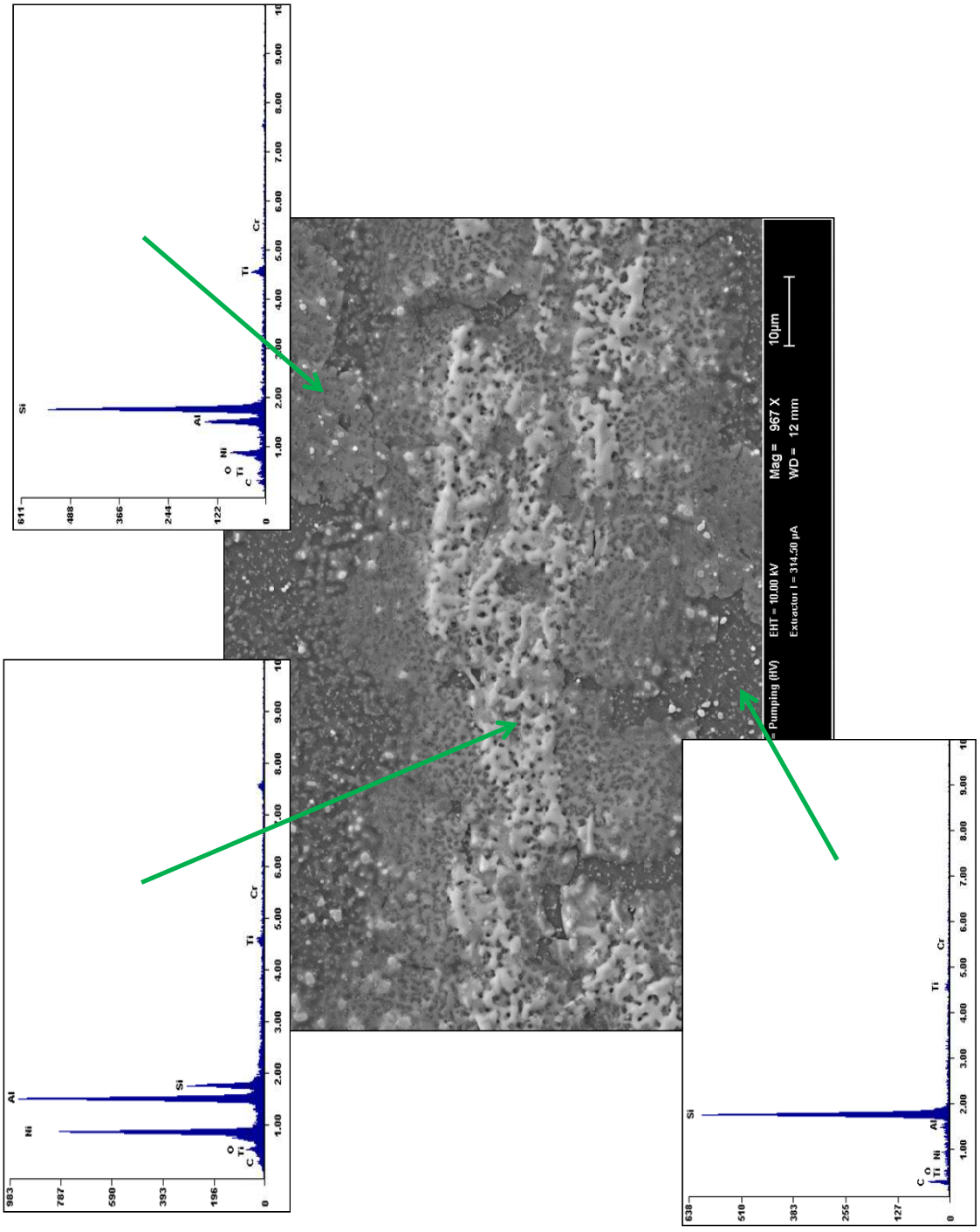


Figure 6.16: SEM image and associated EDAX analysis of annealed Ti/Al/NiV ohmic contact.

6.2.4 XRD Analysis

As well as TEM analysis, XRD analysis has been undertaken on both the unannealed and annealed Al/Ti/Al and Ti/Al/NiV metal contacts, the purpose of which was to identify any metallic phases that have been formed at the metal-semiconductor interface and subsequently assess their relationship with the electrical characteristics of the ohmic contact structures. Figure 6.17 shows the XRD spectra for the Al/Ti/Al metal scheme for a range of annealing conditions as well as the XRD spectra for an unannealed "as-deposited") sample. It can be seen that the XRD spectra for the unannealed sample reveals intense peaks for crystalline 4H-SiC and less intense peaks for the individual metals that were initially deposited, as expected. No peaks representing Ti- or Al-based alloys were identified in the unannealed sample, which was also in line with expectations.

For the formation of Ti/Al-based ohmic contacts to p-type 4H-SiC, the presence of Ti_3SiC_2 is generally accepted for lowering the Schottky barrier at the metal/semiconductor interface, and is thus synonymous with low specific contact resistivity values [120]. As such, this SiC alloy was of particular interest when analysing the XRD spectra. The peaks associated with Ti_3SiC_2 are identified on Figure 6.17; it is evident that this alloy was formed on all of the annealed samples, though the most prominent peaks were on the XRD spectra for the sample annealed at 1000°C for 4 minutes. Because the results of the electrical characterisation showed that the 1000°C 4 minute annealed samples exhibited the lowest specific contact resistance of all of the Al/Ti/Al samples, it seems apparent that an increased presence of Ti_3SiC_2 correlates with lower resistance ohmic contacts. However, it is noted that although the presence of Ti_3SiC_2 was detected to a lesser degree in the remaining annealed samples, the electrical measurements of these samples showed that they did not have ohmic characteristics. As discussed in Section 6.2.2, this is attributed

to the oxidation of Al during the metallisation process.

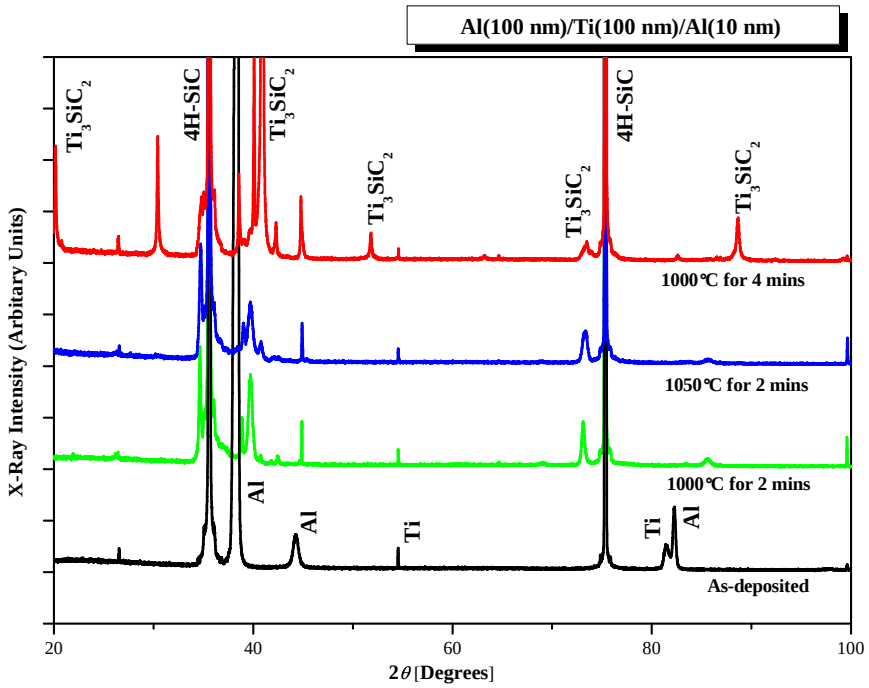


Figure 6.17: XRD spectra of the Al/Ti/Al metal schemes for a range of annealing conditions. For comparison, the XRD spectra for the unannealed sample is also shown.

The XRD spectra for the Ti/Al/NiV samples for a range of annealing conditions is shown in Figure 6.18. As was shown in the XRD spectra for the Al/Ti/Al metal schemes, an annealing temperature of 1000°C was found to be the optimum for the formation of the Ti_3SiC_2 alloy. From analysis of the peaks in the XRD spectra, after a 2 minute anneal at 1000°C the formation of Ti_3SiC_2 was much more pronounced than in the Al/Ti/Al metal scheme, suggesting that when using Ti as the first metal layer, the epitaxially-orientated arrangement with the 4H-SiC prior to annealing (shown in Figure 6.11) is beneficial for forming Ti_3SiC_2 at the metal-semiconductor interface. From inspection of Figure 6.7 it is evident that the improved formation of Ti_3SiC_2 corresponds to a lower specific contact resistance, in accordance with expectations.

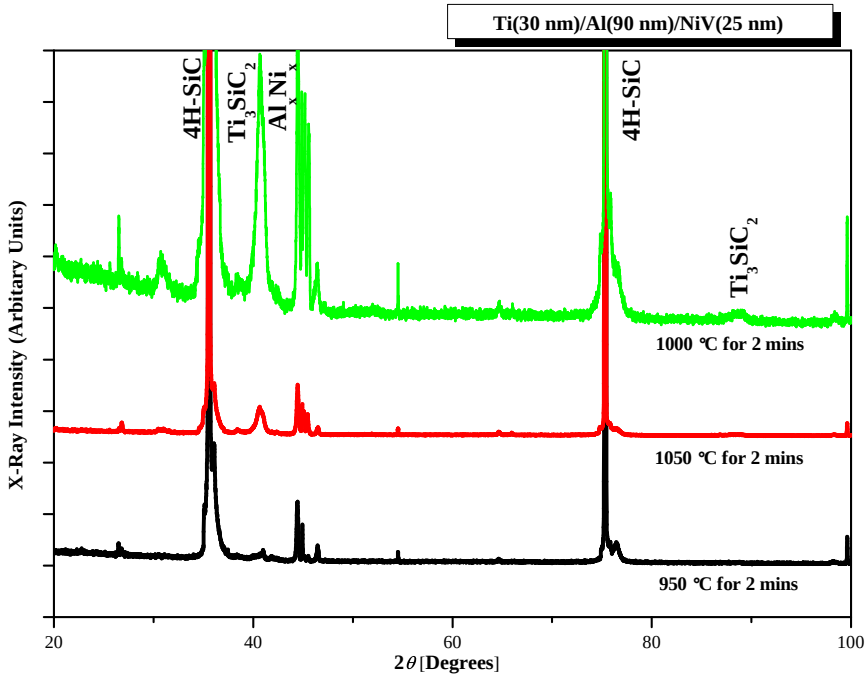


Figure 6.18: XRD spectra of the Ti/Al/NiV metal schemes for a range of annealing conditions.

6.2.5 Current Transport Mechanisms in P-type Ohmic Contacts

In order to quantitatively evaluate the Schottky barrier height lowering effect of Ti_3SiC_2 in each of the fabricated ohmic contact metal schemes, some additional electrical characterisation and analysis has been undertaken. By experimentally determining the dependence of the specific contact resistance on the measurement temperature, an insight into the current transport mechanisms can be obtained [157]. The classical theory for current transport in metal-semiconductor contacts states that the dominant current transport mechanism is dependent on the doping concentration in the semiconductor (N_A), and is

related to a characteristic energy E_{00} described by [119]

$$E_{00} = \frac{h}{4\pi}\sqrt{\left(\frac{N_A}{m^*\varepsilon_S}\right)} \tag{6.1}$$

where h is Planck's constant, m^* is the effective mass of a hole and ε is the dielectric constant of 4H-SiC. This dependence of E_{00} on N_A in 4H-SiC is shown diagrammatically in Figure 6.19 [2]. It is evident from this Figure that for the 4H-SiC samples doped p-type at around 1×10^{19} cm^{-3} used in this ohmic contact study, it is expected that thermionic field emission (TFE) is the dominant current transport mechanism.

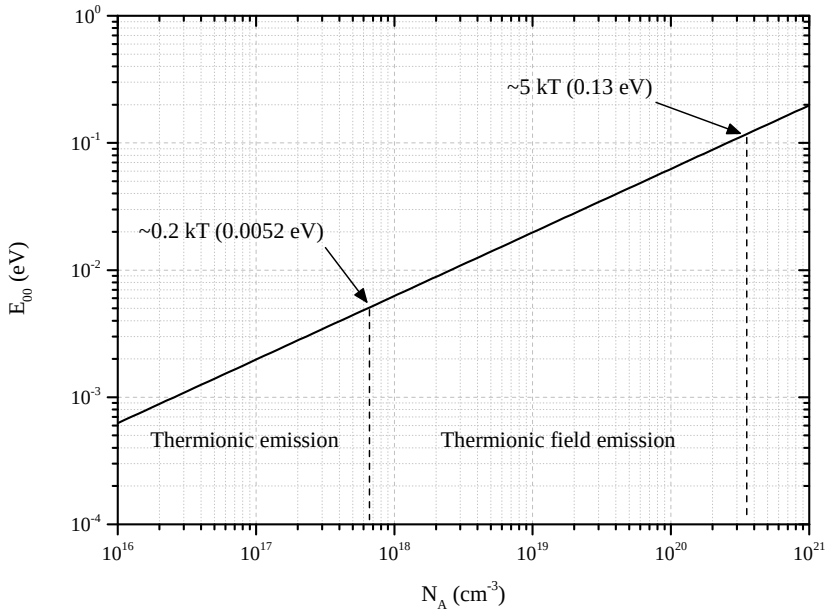


Figure 6.19: Dependence of E_{00} on N_A in 4H-SiC. Though not shown here, field emission dominates beyond the thermionic field emission region ($E_{00} > 0.13$ eV).

According to the TFE model presented in [119], the specific contact resistance can be

expressed as

$$\rho_c = \left(\frac{kT}{qA^*}\right) \frac{kT}{\sqrt{\pi(\Phi_B + V_n)E_{00}}} \cosh\left(\frac{E_{00}}{kT}\right) \left[\sqrt{\coth\left(\frac{E_{00}}{kT}\right)}\right] \exp\left(\frac{\Phi_B + V_n}{E_0} - \frac{V_n}{kT}\right) \tag{6.2}$$

where

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT}\right) \tag{6.3}$$

In Equation 6.2, A^* is the Richardson constant, Φ_B is the Schottky barrier height and V_n is the energy difference between the conduction band edge and the Fermi level. When using this TFE model to fit the experimental data for the range of fabricated p-type ohmic contacts, both Φ_B and N_A have been used as fit parameters. It was considered important to use N_A as a fitting parameter because although a value for N_A of $>1\times10^{19}$ cm^{-3} was specified to the epitaxial material supplier, the value is likely to depart from this due to incomplete ionisation as well as the control of the doping during the epitaxial growth process. The fitting calculations have used values of $\varepsilon_S = 9.7\varepsilon_0$ (where ε_0 is the vacuum permittivity), A^*=146 A/cm^2-K^2 and $m^* = 0.91m$ (where m is the electron mass) [158], and have been performed using the Curve Fitting Toolbox in MATLAB [159].

Figure 6.20 shows the dependence of specific contact resistance on measurement temperature for the Al/Ti/Al ohmic contacts. Because the contacts annealed at 1000°C and 1050°C for 2 minutes both exhibited rectifying characteristics, only the contact annealed at 1000°C for 4 minutes is shown. From fitting to the experimental data across the measurement temperature range, a Schottky barrier height of 0.54 eV was extracted from fitting to the TFE model. Similarly, the specific contact resistance as a function of measurement temperature for the Ti/Al/NiV ohmic contacts is shown in Figure 6.21. In this Figure, a logarithmic y-axis has been used in order to provide a comparison of the

Ti/Al/NiV contacts across the range of annealing temperatures. Corresponding to the higher measured specific contact resistance of the sample annealed at 950°C for 2 minutes, this sample was found to have the highest Schottky barrier height, at 0.56 eV. Though not stated on the Figure, the samples annealed at 1000°C and 1050°C were found to have Schottky barrier heights of 0.51 eV and 0.54 eV respectively.

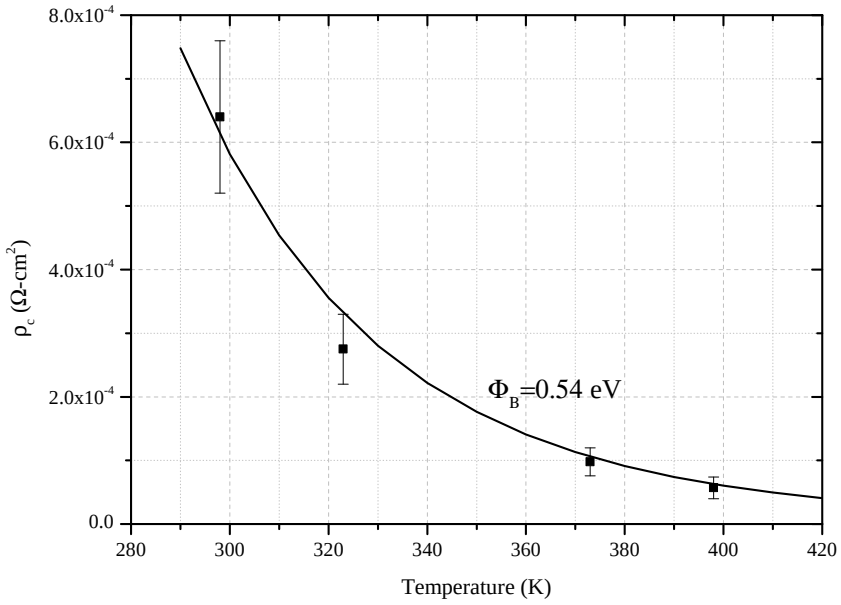


Figure 6.20: Contact resistance as a function of measurement temperature for Al/Ti/Al ohmic contacts.

When compared against the other Ti/Al/NiV ohmic contact samples, the sample annealed at 1000°C for 2 minutes with a pre-anneal at 600°C for 2 minutes exhibited a considerably lower specific contact resistance, and, correspondingly, a lower Schottky barrier height, found to be 0.43 eV. Though this could be thought to be due to the longer overall anneal duration, it can be seen from Figure 6.8 that the 4 minute anneal at 1000°C yielded a mean specific contact resistance of around 4×10^{-4} Ω-cm^2, considerably

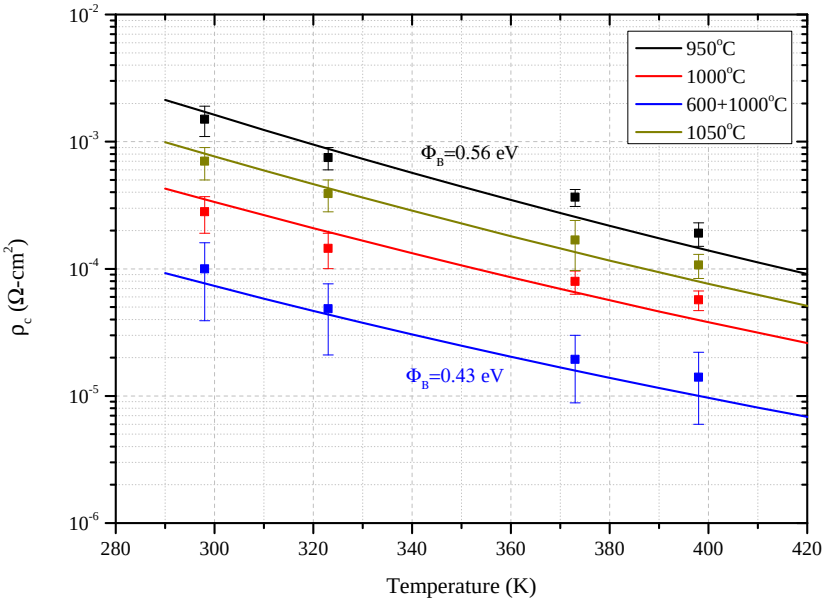


Figure 6.21: Contact resistance as a function of measurement temperature for Ti/Al/NiV ohmic contacts. Data for the range of annealing temperatures is shown (all anneals were for 2 minutes, except the 600°C+1000°C process, which was for 2 + 2 minutes).

higher than that for the sample with the 2 minute 600°C pre-anneal. This suggests that the pre-anneal at 600°C promotes the formation of Schottky barrier-lowering silicides at the metal-semiconductor interface [160]. Though not shown here, fitting of the specific contact resistance across the measurement temperature range of the Ti/Al/NiV samples annealed at 1000°C for 1 and 4 minutes both indicated that a Schottky barrier height of 0.54 eV was present. Finally, Figure 6.22 shows the dependence of specific contact resistance on measurement temperature for the Ti/Al ohmic contacts annealed at 1000°C for 2 minutes with a 2 minute pre-anneal at 600°C. As expected from the lower specific contact resistance of this metal scheme, the Schottky barrier height was lower than the previously-measured samples, at 0.32 eV.

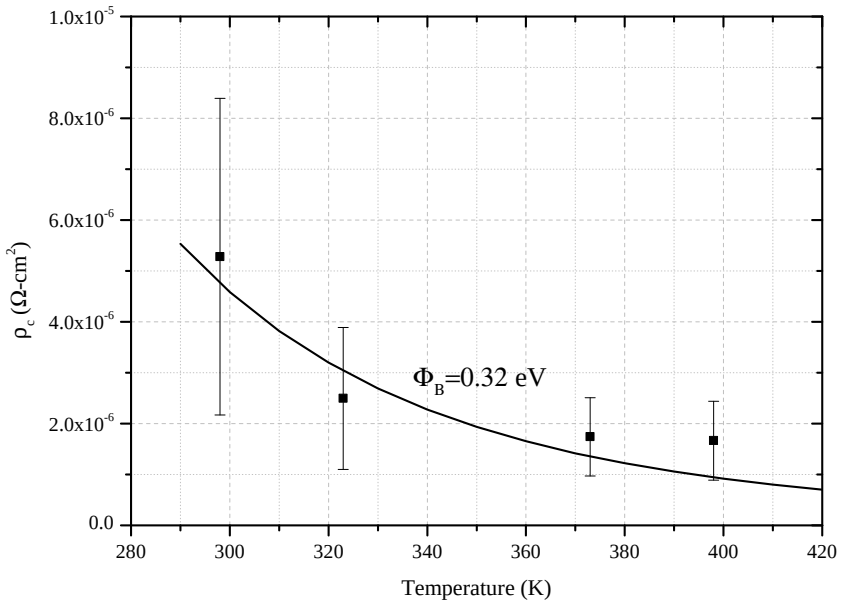


Figure 6.22: Contact resistance as a function of measurement temperature for Ti/Al ohmic contacts.

6.3 Benchmarking of P-type Ohmic Contact Results

In order to put the experimental results achieved in this Chapter into context, it is useful to compare them to results obtained by the wider research community. As such, Table 6.3 provides a comprehensive list of results for p-type 4H-SiC ohmic contact resistance, including the results presented in this Chapter. It is evident that the results obtained in this Chapter compare favourable to those published elsewhere. However, a more critical review would investigate the stability of these ohmic contacts over time; to date, very little data is available on this subject.

Table 6.3: Comparison of p-type ohmic contact specific contact resistance. All results presented are for epitaxial 4H-SiC material.

Metal	N_A (cm^{-3})	Annealing	ρ_C (Ω-cm^2)	Ref.
Al(100 nm)/Ti(100 nm)/Al(10 nm)	$>10^{19}$	4 min at 1050°C in Ar	2.8×10^{-4}	This work
Ti(30 nm)/Al(90 nm)/NiV(25 nm)	$>10^{19}$	2 min at 600°C + 2 min at 1000°C in Ar	3.7×10^{-5}	This work
Ti(30 nm)/Al(90 nm)	$>10^{19}$	2 min at 600°C + 2 min at 1000°C in Ar	2.2×10^{-6}	This work
Ti(60 nm)/Al(140 nm)	10^{19}	2 min at 1000°C in vacuum	4.9×10^{-5}	[161]
Ni(25 nm)/Ti(50 nm)/Al(300 nm)	3×10^{18}	30 min at 800°C in vacuum	6.6×10^{-5}	[162]
Ge(24 nm)/Ti(32 nm)/Al(144 nm)	4.5×10^{18}	30 min at 600°C in vacuum	1×10^{-4}	[163]
Al/Ti (31 wt% Ti)	4.8×10^{18}	2 min at 1000°C in vacuum	2.5×10^{-4}	[118]
Au(100 nm)/Ti(70 nm)/Al(30 nm)	3×10^{19}	900°C in Ar + 1% H_2 gas	1.42×10^{-5}	[164]
Ni(10 nm)/Ti(40 nm)/ Al(240 nm)/Ni(10 nm)	3×10^{19}	90s at 800°C in Ar	1.5×10^{-5}	[165]
Al(100 nm)/Ti(100 nm)/Al(10 nm)	10^{19}	5 min at 1050°C in Ar	5×10^{-6}	[3]

6.4 Summary

In this Chapter, the development of two key fabrication processes required for realising high voltage 4H-SiC PiN diodes, dry etching and p-type metallisation, have been presented. The investigation into the use of ICP and RIE-based etching processes was first discussed, and details of the etch rates and selectivity for the range of different etch process required for device fabrication were outlined. The etching of SiO_2 was investigated first; this initially proved problematic due to the photoresist mask being heat damaged during the ICP etch process. In order to circumvent this problem, a NiV mask was used instead of photoresist; this yielded significantly better feature definition. An alternative solution that was suggested was to use a RIE process instead of an ICP process, as this lower power etch did not result in any degradation of the photoresist mask. However, this alternative came at the expense of a longer etch duration. Etching of 4H-SiC was found to require an ICP-based process in order to achieve a practical etch rate, and the use of a NIV masking layer was most effective in providing a satisfactory level of selectivity.

After this investigation into ICP / RIE processing, a study into the formation of ohmic contacts to p-type 4H-SiC was presented. The fabrication process that was used to realise the TLM structures used for electrical analysis of the various metal schemes was first outlined, along with the geometrical details of the TLM structures. The electrical characterisation results of the fabricated TLM structures were presented next; the first metal scheme that was investigated was Al/Ti/Al. Although excellent results for this metal scheme were presented in the literature [3], the electrical characterisation in the investigation undertaken in this Chapter showed that this metal scheme suffered from rectifying behaviour for anneals of 2 minutes duration at both 1000°C and 1050°C, though by increasing the anneal duration to 4 minutes, ohmic behaviour was observed with a specific

contact resistance of 2.8×10^{-4} Ω-cm^2. This poor electrical performance was attributed to oxidation of Al during the metal deposition, a by-product of an insufficiently low base pressure during the process.

Next, metal contacts using a Ti-initial layer were electrically characterised, and, overall, were found to have considerably lower specific contact resistances than the previously investigated Al/Ti/Al structures. For the Ti/Al/NiV structure, a specific contact resistance less than 4.0×10^{-5} Ω-cm^2 was measured; this was achieved after annealing at 600°C followed by 1000°C for 2 minutes at each temperature. However, it was found that poor adhesion of the NiV layer occasionally caused the metal to peel off during the lift-off process used for contact definition. As a result of this, the NiV layer was removed from subsequent metal schemes; this enabled the lowest specific contact resistance of 2.2×10^{-6} Ω-cm^2 to be achieved.

After the electrical characterisation of the metal contacts was completed, physical analysis was performed in order to obtain an understanding of the mechanisms governing the performance of the fabricated contact structures. TEM analysis of an unannealed Ti/Al/NiV sample showed that the Ti was deposited epitaxially onto the 4H-SiC, as a result of the similar lattice constants of the two materials. The Al was shown to have a polycrystalline structure, whilst the NiV appeared to be amorphous. In addition, a thin layer of SiO_2 between the Al and the NiV layers was observed, this perhaps explains the poor adhesion of the NiV that was encountered during processing. TEM analysis of an annealed Ti/Al/NiV contact structure showed that the contact morphology had significantly departured from that of the unannealed sample; only an inhomogeneous Ti-based layer was evident. Moreover, the 4H-SiC/Ti interface no longer appeared to have the epitaxial relationship that it did prior to annealing. The presence of Al was no longer obvious from the TEM analysis, due to the high annealing temperature; this was backed

up by SEM / EDAX analysis of the contact structure.

Performing XRD analysis showed that the formation of the Ti_3SiC_2, a metallic phase that has been found to be effective in lowering the Schottky barrier height at the metal-4H-SiC interface and thus reducing the specific contact resistance, was observed over the complete range of annealed samples, and was more prominent in metal schemes that had exhibited the lowest specific contact resistance values. By analysing the current transport mechanisms in the ohmic contact structures, this relationship between the Ti_3SiC_2 formation and the specific contact resistance of was also found to correlate with the Schottky barrier height, with the best performing ohmic contact (Ti/Al) having both the lowest mean value of specific contact resistance of around 5.3×10^{-6} Ω-cm^2 and the lowest Schottky barrier height of 0.32 eV.

Chapter

7 Fabrication and Characterisation of 3.3 kV 4H-SiC PiN Diodes

In this Chapter, the fabrication and characterisation of 4H-SiC PiN diodes targeting 3.3 kV blocking voltage is presented. First, details of the photomask design and epitaxial structures of the PiN diodes are presented. Following this, a discussion of the fabrication process and the electrical characterisation results for the 3.3 kV PiN diodes is given, which follows the chronological evolution of these devices. First generation devices have been fabricated using a simple process without edge termination, and the forward and low-voltage reverse I-V characteristics of these devices are analysed in detail. The second generation PiN diodes have been fabricated with edge termination, thus facilitating the same electrical characterisation as the first generation devices, as well as an analysis of reverse breakdown performance. In addition to the electrical characterisation, results of physical characterisation of ion implanted edge termination structures is presented, which complements the electrical results that are presented.

7.1 Photomask Design

In order to enable fabrication of the high voltage 4H-SiC PiN diodes, a set of mask plates have been designed using Tanner Tools' L-Edit software [166] and manufactured at Compugraphics, UK [167]. The design of a single 14×14 mm die, which is duplicated across a three inch wafer mask, is shown in Figure 7.1. This die is labelled "DIE6"; the mask design contains nine different dies, each with different device active areas (two large and two small). On each die, in addition to the four PiN diode devices, are TLM structures for ohmic contact measurements, and van der Pauw structures for measuring the sheet resistance, and thus doping concentration, of the implanted regions of the devices. It can also be seen from Figure 7.1 that there is a 1.5 mm exclusion region at the periphery of the die; this has been incorporated so that any photoresist build-up at the edges of the sample can be removed by exposing through a specifically designed 'edge-bead removal' mask plate which covers the all of the features on the die (not shown here for clarity).

7.2 Device Structures

The 4H-SiC material for these devices was obtained from Dow Corning [34]. In order to maximise device yield from these substrates, 'prime grade' material with a micropipe density of less than 1 per cm^2 was specified. Epitaxial layers were grown in a continuous growth run in an Aixtron VP-508 single-wafer reactor at Norstel [32]; the epitaxial structures that were specified are illustrated in Figure 7.2. After epitaxial growth, the wafers have been laser-cut into 14×14 mm chips for subsequent processing. The dimensions of the devices that have fabricated are outlined in Table 7.1.

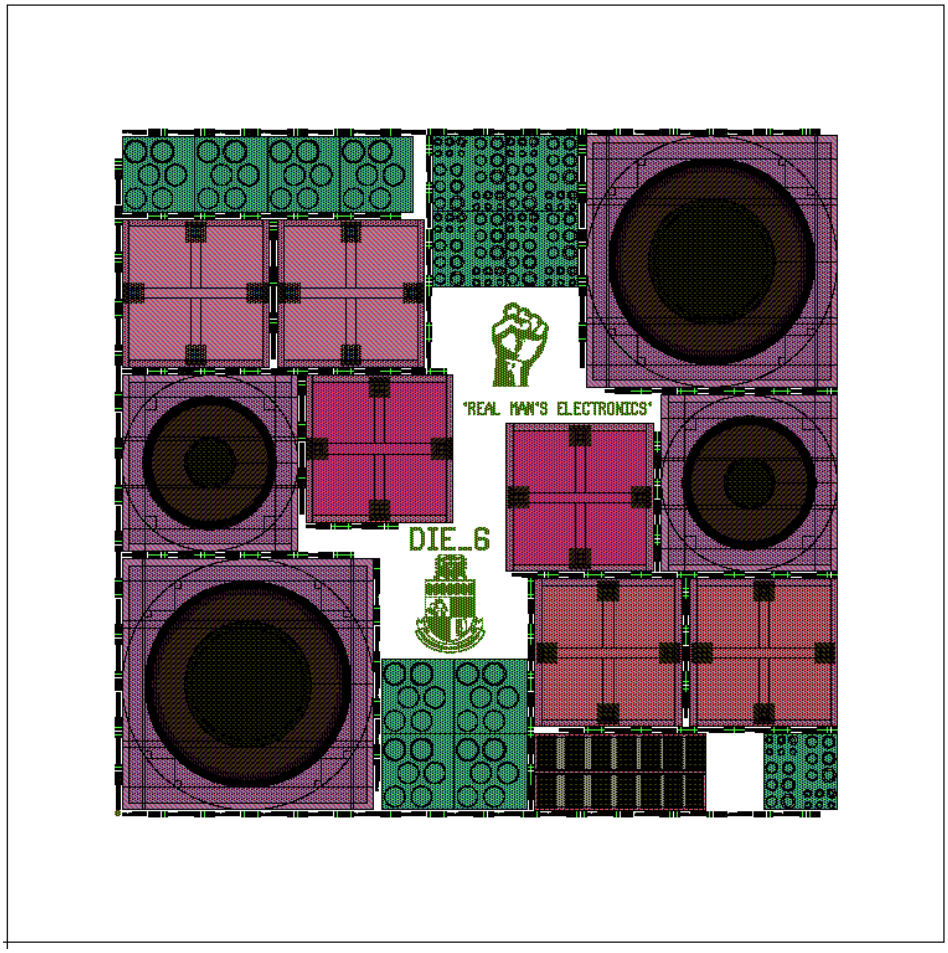


Figure 7.1: Die design for PiN diode fabrication (DIE6 shown in this image).

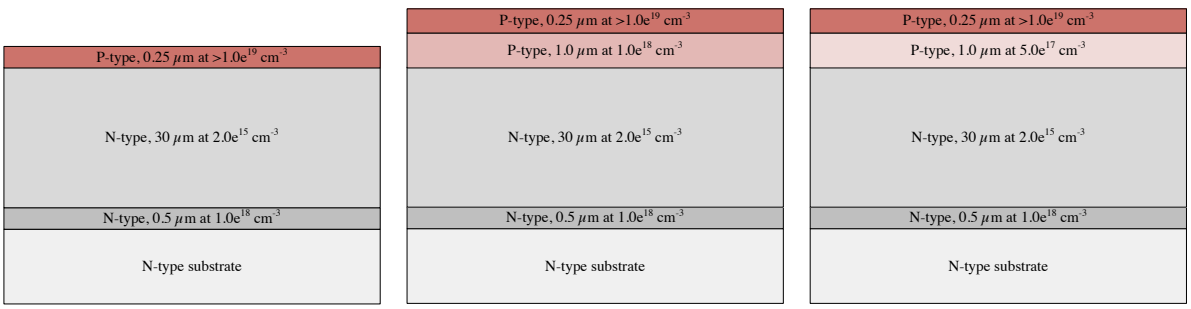


Figure 7.2: Epitaxial structures of 3.3 kV 4H-SiC PiN diodes (from left to right, sample IDs are: PiN1, PiN2 and PiN3).

7.3 First Generation 4H-SiC PiN Diodes

The initial iteration of 4H-SiC PiN diodes discussed in this Section have been fabricated with a simplified process, without the JTE implantation. Though this means that these initial devices do not have the capability to to block the intended voltage of 3.3 kV, their forward I-V performance, reverse leakage current and switching characteristics can still be evaluated, and used as a benchmark for future device iterations. In this first generation of PiN diodes, 8 devices have been fabricated (2 dies).

Table 7.1: Dimensions of first generation 3.3 kV PiN diodes.

Device size	Active area (cm^2)	Anode perimeter (cm)	P/A ratio
DIE3 (large)	0.0177	0.471	26.7
DIE3 (small)	0.0011	0.118	107

7.3.1 Fabrication Process

The first process in the PiN diode fabrication was the cleaning of the 4H-SiC samples, according to the procedure outlined in Appendix B. Following this, one micron of TEOS oxide was deposited on the samples; this served as the mesa etch mask. A further 100 nm of NiV was sputtered onto samples PiN2 and PiN3 due to the deeper SiC etch required to isolate the thicker epitaxial anode. Using the standard photolithography process described in Appendix C, the active areas of the devices were patterned onto the sample surface. The NiV was etched using Aqua Regia solution (hydrochloric acid (HCl), nitric acid (HNO_3) and DI water in the ratio 5:1:6), then the exposed TEOS oxide was etched using the ICP etch process discussed in Chapter 6 to obtain a vertical sidewall profile. Following this, the photoresist was removed in an O_2 plasma, then the exposed SiC was etched to the required depth (∼500 nm greater than the anode thickness) to mesa-isolate the individual

device anodes. After SiC etching, the remaining TEOS oxide was removed in 10% HF solution.

The next process was the passivation and metallisation of the top (p-type) SiC surface; this was achieved by first depositing one micron of TEOS oxide on the top surface of the samples. After carrying out a second standard photolithography process, the TEOS oxide was etched in the regions of the mesa-isolated anodes to a depth of ∼800 nm using RIE. The remaining ∼200 nm of TEOS oxide was then etched away through to the SiC surface using 10:1 buffered oxide etch (BOE), and the samples were rinsed in DI water. Next, a Ti/Al/NiV ohmic contact to the p-type anode was sputtered onto the sample, and the unwanted metal and photoresist was removed via an ultrasonic lift-off process in acetone.

After the p-type metallisation process, the next step was to metallise the backside (n-type cathode) of the devices. Firstly, the residual backside oxide was removed using an ICP etch, then a Ti/NiV ohmic contact was blanket-sputtered onto the back surface of the samples. Once the backside metallisation was complete, the samples were annealed in an RTA furnace at 600°C for 2 minutes then at 1000°C for a further 2 minutes, in an argon atmosphere. This level of processing was sufficient to enable the characterisation of forward and reverse I-V performance (up to 100 V) of the devices on a probe station.

7.3.2 Forward I-V Characterisation Results

In this Section, the forward I(J)-V, characteristics are presented for the first generation of fabricated PiN diodes. The on-state behaviour of these devices has been evaluated by means of forward I-V measurements at room temperature, in addition to measurements of test structures on the semiconductor dies. From these measurements, the diode ideality factor (η), differential on-resistance ($R_{on,diff}$) and reverse saturation current density

(J_0) of the devices have been extracted, which has allowed a detailed analysis of the performance of the fabricated PiN diodes.

The log(J)-V characteristic of a selected small-area PiN1 diode at 25°C is illustrated in Figure 7.3. From this characteristic, each of the forward bias operational modes of the PiN diode can be explained. At low forward bias the J-V characteristic is dominated by recombination current, which is proportional to the intrinsic carrier concentration n_i. For a P+/N- junction (where the hole concentration in the n-type semiconductor in equilibrium is greater than the electron concentration in the p-type semiconductor) and when $V_A \gg kT/q$, the total forward current can be approximated by [42]

$$J_F = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D}\exp\left(\frac{qV_A}{kT}\right) + \sqrt{\frac{\pi}{2}}\frac{kTn_i}{\tau_p \mathscr{E}_o}\exp\left(\frac{qV_A}{2kT}\right) \tag{7.1}$$

where $\mathscr{E}_o$ is the electric field at the location of maximum recombination. All other parameters have been defined previously in Chapter 3. The experimental J-V results for the PiN diode can be represented by the empirical form

$$J_F \propto \exp\left(\frac{qV}{\eta kT}\right) \tag{7.2}$$

In the region where recombination current dominates, the ideality factor η is equal to 2. As the forward bias increases and approaches the diode built-in voltage, given by

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{7.3}$$

diffusion current begins to dominate and, beyond the built-in voltage, η is equal to 1. When both currents are comparable, η has a value between 1 and 2. When the forward bias is higher still, recombination current in the diode again dominates due to the high-

level of injected carriers in the drift region, and η is equal to 2. Finally, the current conduction in the diode is limited by the series resistance of the device, which is comprised of not only the semiconductor but also the ohmic contacts and the wire bonding and packaging (assuming the device is packaged). It is noted that the high-level injection regime is difficult to observe from Figure 7.3, due to the series resistance of the diode quickly dominating the J-V characteristic.

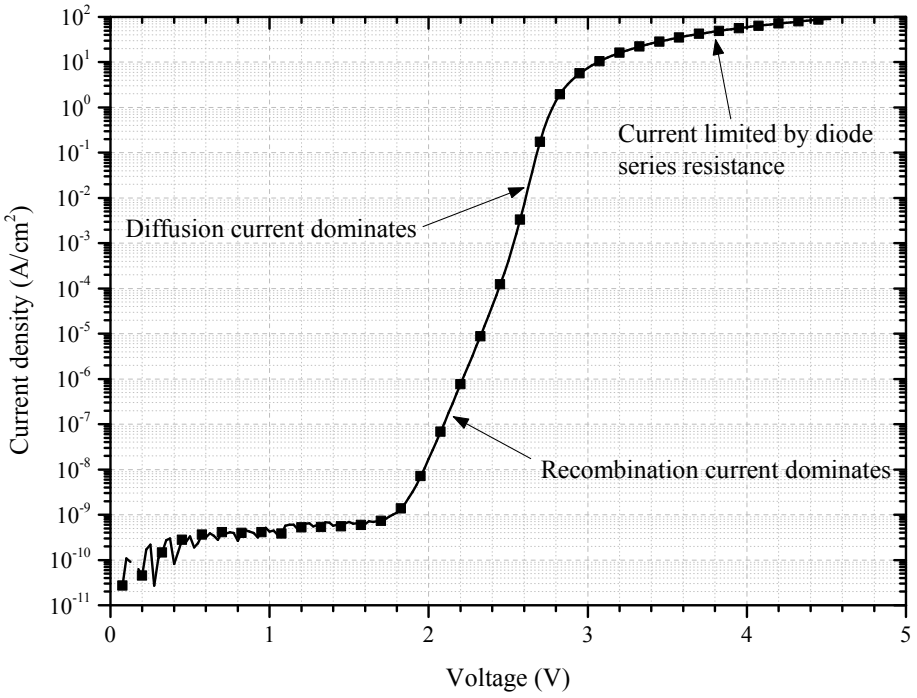


Figure 7.3: Forward log(J)-V characteristic of a selected small-area first generation 3.3 kV 4H-SiC PiN1 diode at 25°C. The dominant current conduction mechanisms for each section of the diode J-V characteristic are also illustrated.

Though the power limitations of the measurement equipment meant that the small-area devices could only be tested up to a maximum current density of approximately 90 A/cm^2, extrapolating the device J-V characteristic gives a voltage drop of approxi-

mately 4.8 V at 100 A/cm^2. The differential on-resistance of the device, given by

$$R_{on,diff} = \frac{dV(J_F)}{dJ_F} \tag{7.4}$$

was found to be 17 mΩ-cm^2 at 100 A/cm^2 and 25°C, and is illustrated as a function of current density in Figure 7.4. It can be seen that $R_{on,diff}$ is initially high, as at low forward bias the resistive drift region is unmodulated, then as the conductivity modulation begins to take effect the resistance of the device decreases.

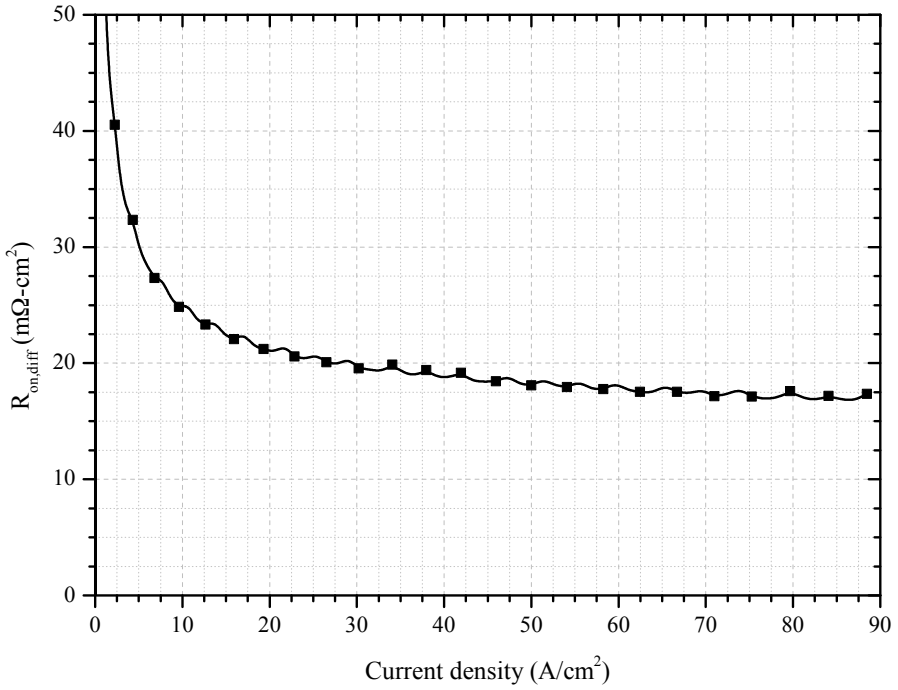


Figure 7.4: Differential on-resistance against current density of a selected small-area first generation 3.3 kV 4H-SiC PiN1 diode at 25°C.

Next, the ideality factor of the fabricated diodes was calculated from the experimental data. This calculation is based on the ideal diode equation, given by

$$J_F = J_0 \left(e^{\frac{qV_A}{\eta kT}} - 1 \right) \tag{7.5}$$

in which

$$\eta = \frac{1}{S\frac{kT}{q}\ln(10)} \tag{7.6}$$

and

$$S = \frac{d\log(J_F)}{dV_F} \tag{7.7}$$

Figure 7.5 shows the ideality factor η of a fabricated small-area PiN1 diode against forward voltage in the turn-on region. It is evident that prior to turn-on (below ∼2.4 V), in the recombination current region, the ideality factor is around 2, as expected. After turn-on, the ideality factor drops to around 1.3, slightly above the ideal value of $\eta = 1$. As such, it can be inferred that, in addition to diffusion, recombination centres play an active role in the current transport in the PiN diodes. It can also be seen that, due to the high series resistance of the diode, the ideality factor increases significantly with increasing forward bias.

The forward log(J)-V characteristics of the PiN diode can also be used to estimate the effective carrier lifetime in the device, by utilising the saturation recombination current density, $J_{0,rec}$, in conjunction with the equation for forward recombination current of a *pn* diode [168]

$$J_{rec} = \frac{qW_D n_i}{2\tau_e} \exp\left(\frac{qV}{2kT}\right) \tag{7.8}$$

where W_D is the width of the drift region, n_i is the intrinsic carrier concentration and τ_e is the effective carrier lifetime. By extrapolating to $V = 0$ whilst maintaining the

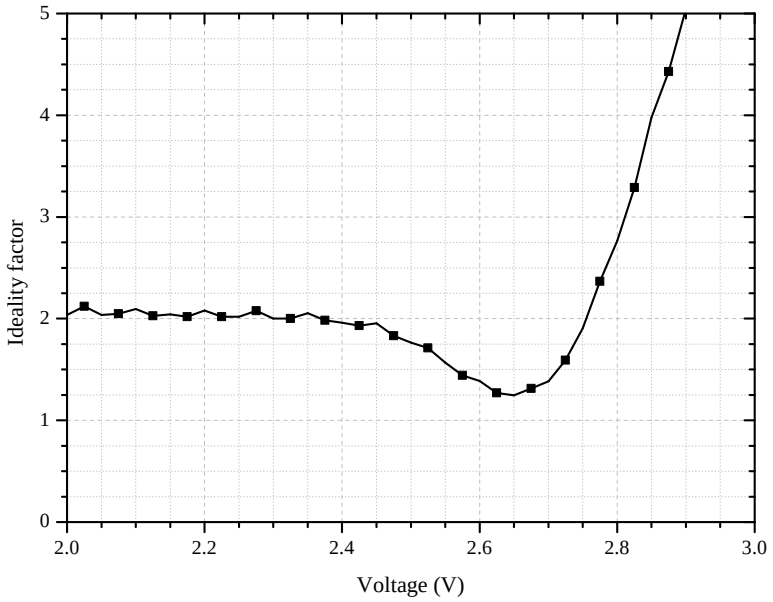


Figure 7.5: Ideality factor against voltage of a selected small-area first generation 3.3 kV 4H-SiC PiN1 diode at 25°C.

recombination current region ideality factor of $\eta \approx 2$, Equation 7.8 simplifies to

$$J_{0,rec} = \frac{qW_D n_i}{2\tau_e} \tag{7.9}$$

which can be rearranged to yield the effective carrier lifetime such that

$$\tau_e = 0.5 \cdot \left(\frac{qW_D n_i}{J_{0,rec}} \right) \tag{7.10}$$

Therefore, by experimentally determining the value of $J_{0,rec}$, the effective carrier lifetime can be estimated. At 300 K, for $J_{0,rec} = 5 \times 10^{-24}$ A/cm^2 (typical measured value), $n_i = 5 \times 10^{-9}$ cm^{-3} [103], the effective carrier lifetime is estimated to be 480 ns, which is typical of the value expected from as-grown 4H-SiC material.

7.3.3 Reverse I-V Characterisation Results

Using the same measurement equipment as for the forward I-V characterisation, the reverse I-V characteristics of the diodes were measured up to 100 V, with the results presented in Figure 7.6. From these results, it is evident that the value of reverse leakage current density at the maximum bias voltage of 100 V varies by approximately seven orders of magnitude, from 5 nA/cm^2 up to 200 μA/cm^2 at 25°C. This equated to a geometric mean value μ_g of 259 nA/cm^2 and standard deviation σ_g of 46.97 for the complete set of data. Since all of these devices underwent identical processing steps, it was considered likely that the defects in the semiconductor material are the predominant cause of this large variation. However, because of the inherently variable nature of a research cleanroom facility, variations in the processing conditions cannot be ruled out. The abrupt, high reverse leakage current profiles of the large-area devices L-A_2 and L-A_4 suggest that these two devices are compromised by micropipe or triangular defects, highlighting the problems faced in 4H-SiC device fabrication, even when low micropipe density substrates are used.

7.3.4 The Impact of a Metal Overlayer on Forward I-V Characteristics

In order to enable the fabricated PiN diodes to be wire-bonded and packaged, a thick ($\sim$1 μm) Al layer with a contact diameter of 2 mm needs to be deposited onto the top side of the die, thus covering the ohmic contact layer and extending over the passivated mesa periphery. The use of Al and the size of the contact pads were chosen to be compatible with the wire bonding equipment used in this work. However, as shown in Figure 7.7, which shows the J-V characteristics of two small-area PiN diodes before and after the

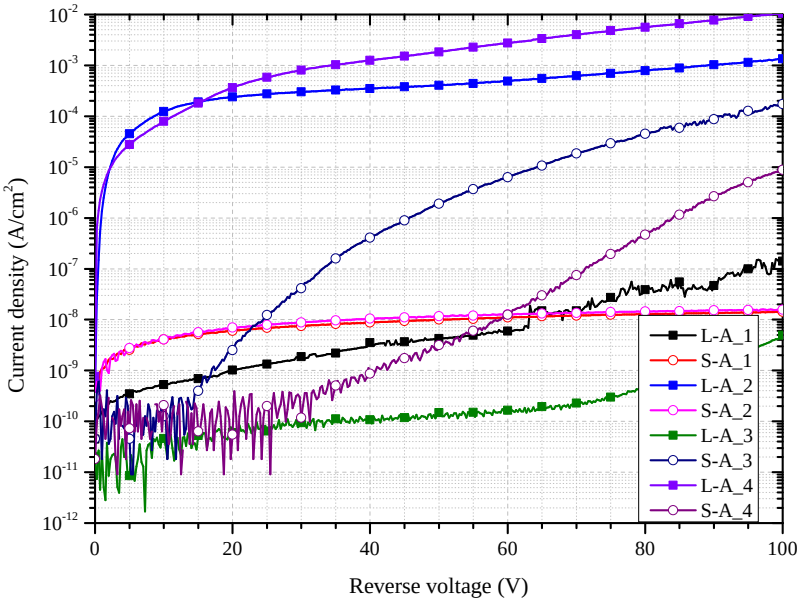


Figure 7.6: Reverse log(J)-V characteristics of first generation 3.3 kV 4H-SiC PiN diodes at 25°C. L-A and S-A refer to large- and small-area devices respectively.

metal overlay process, the device characteristics were found to be significantly affected by this process. Though the use of the metal overlay has resulted in a considerable lowering of the specific on-resistance of the devices under high-level injection conditions, which from a practical perspective is beneficial, it has also introduced a conduction path in parallel with the main *pn* junction, resulting in high (>2) ideality factors in the low current regime. This behaviour can be modelled by including a Schottky diode with its own series resistance in parallel with the main *pn* junction [169].

An interesting observation from this investigation into the use of a metal overlay was that the impact on the J-V characteristics of the large-area PiN diodes was minimal in comparison to the previously-shown small-area devices. An example of the forward J-V characteristics for a large-area device before and after the deposition of the metal

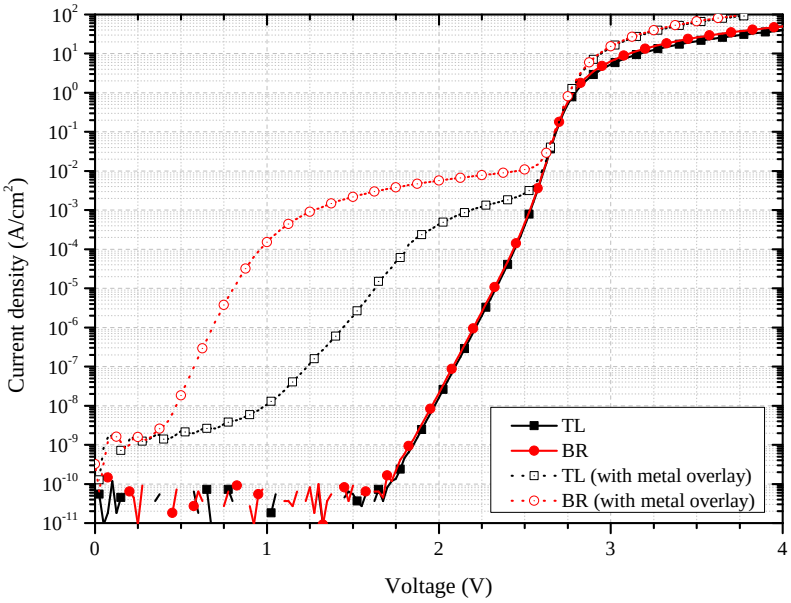


Figure 7.7: Comparison of Forward log(J)-V characteristic of small-area first-generation 3.3 kV 4H-SiC PiN1 diodes with and without metal overlayer at 25°C. The abbreviations 'TL' and 'BR' refers to the top left and bottom right locations of PiN diodes on the same fabricated die.

overlay is shown in Figure 7.8. Though the leakage current is approximately one order of magnitude higher for the device with the metal overlay (which can be attributed to leakage through the TEOS SiO_2 underneath the area of the Al layer), the characteristics in the recombination current and diffusion current regions of the device characteristics are nearly identical across both devices. As with the small-area diodes, the use of the metal overlay was beneficial for reducing the specific on-resistance of the large-area devices under high-level injection conditions.

Because of the correlation between non-ideal J-V characteristics in low forward bias and the high perimeter-to-area ratio inherent of the small-area devices, it is logical to conclude that the parasitic Schottky diode is present at the vertical surface of the mesa

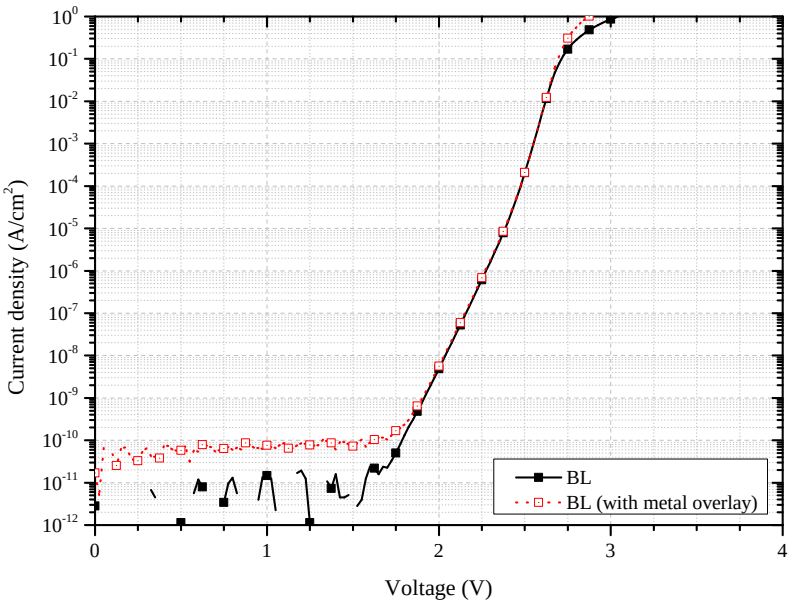


Figure 7.8: Comparison of Forward log(J)-V characteristic of large-area first-generation 3.3 kV 4H-SiC PiN1 diodes with and without metal overlayer at 25°C. The abbreviation 'BL' refers to the bottom left location of PiN diodes on a given die.

etched sidewall, suggesting that the TEOS SiO_2 has not fully passivated this surface. In order to remedy this, either a thicker layer of TEOS SiO_2 (thicker than the depth of the mesa etch) could be used, or an intermediate thermal oxide layer could be grown prior to the deposition of the TEOS SiO_2.

7.4 Second Generation 4H-SiC PiN Diodes

For the second generation of 4H-SiC PiN diodes, the fabrication process outlined in Section 7.3.1 has been extended to include the B-implanted JTE region, with the aim of achieving the targeted blocking voltage of 3.3 kV. A total of 9 samples (36 devices) have been processed for this generation of devices; all of these samples have been taken from the PiN3

epitaxial wafer. Once fabricated, these devices have been characterised both electrically and physically, to evaluate the reverse breakdown voltage capability of the PiN diodes as well as the crystalline structure and doping profile of the implanted regions. The purpose of the physical characterisation is threefold; firstly, SIMS analysis has been undertaken, to verify the implanted doping profiles against the outlined specifications. Secondly, Raman spectroscopy has been applied to determine the effectiveness of various anneal processes used to activate the implanted dopants. Thirdly, AFM has been used to characterise the surface morphology of implanted / annealed samples, to investigate the effectiveness of the capping layers used to minimise step bunching.

7.4.1 Fabrication Process

As with the devices fabricated previously, samples first underwent the cleaning process outlined in Appendix B, and have been mesa etched to isolate the p-type anodes. Following the mesa etch, one micron of TEOS oxide and 300 nm of NiV has been deposited onto the samples to serve as the ion implantation mask. SRIM simulations have been employed to verify that this mask will not be penetrated by the implanted ions at the maximum implant energy of 360 keV, as illustrated in Figure 7.9. After performing the photolithography process described in Appendix C, the JTE implant windows in the NiV and TEOS oxide have been opened up using Aqua Regia solution followed by ICP etching, then the photoresist removed in an O_2 plasma.

In order to obtain a broad range of data and determine the optimum implantation conditions for the JTE, three different implant schemes have been used, as detailed in Table 7.2. All ion implantation processes described in this Section have been carried out at Cutting Edge Ions, LLC [170]. From the simulation results presented in Chapter 4,

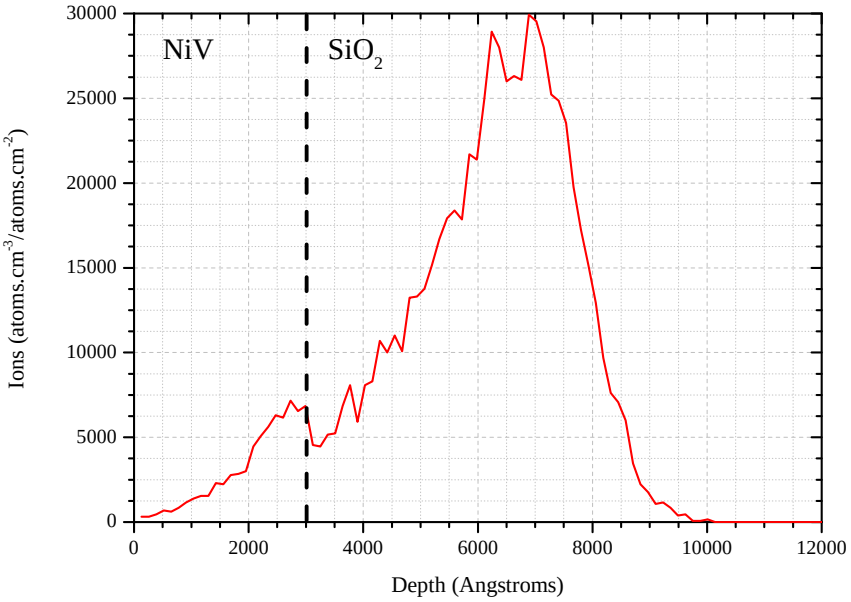


Figure 7.9: Implant profile of boron in NiV/SiO_2 mask at an implant energy of 360 keV (obtained using SRIM simulation software).

the optimum dopant concentration for the JTE region was found to be 1.5×10^{17} cm^{-3}; this has therefore been used as the mid data point, and one data point either side of this has been used. For each implant scheme, five successive implants have been used, to yield an approximate box profile. The simulated implant profile of the mid data point is illustrated in Figure 7.10. It is evident from this Figure that the target implanted dopant concentration is four times higher than the optimum value specified above; this is because a dopant activation rate of 25% has been assumed [76]. Three separate samples have undergone each implant scheme, in order to facilitate the comparison of post-implant annealing conditions between 1500°C and 1700°C. Implants have been performed at a temperature of 650°C, to promote the implanted dopant atoms ending up on substitutional lattice sites [111].

Table 7.2: Ion implantation specifications for 3.3 kV PiN diode JTE, for low-dose (LD), medium-dose (MD) and high-dose (HD) implant schemes.

PiN diode ID	Target dopant concentration (cm^{-3})	Implant energy (keV)	Implant dose (cm^{-2})	Total implant dose (cm^{-2})
PiN3.3.LD	7.5×10^{16}	360	6.5×10^{12}	2.03×10^{13}
		220	5.25×10^{12}	
		120	4.0×10^{12}	
		60	2.75×10^{12}	
		25	1.5×10^{12}	
PiN3.3.MD	1.5×10^{17}	360	1.3×10^{13}	4.0×10^{13}
		220	1.05×10^{13}	
		120	8.0×10^{12}	
		60	5.5×10^{12}	
		25	3.0×10^{12}	
PiN3.3.HD	3.0×10^{17}	360	2.6×10^{13}	8.0×10^{13}
		220	2.1×10^{13}	
		120	1.6×10^{13}	
		60	1.1×10^{13}	
		25	6.0×10^{12}	

After the ion implantation process, the NiV and SiO_2 mask has been removed in Aqua Regia solution and HF solution. The samples then underwent a RCA1 and RCA2 clean, in order to remove any potential metallic compounds present. Following this, the capping layers for the activation anneal were deposited; as discussed in Chapter 3, the capping layer is required to prevent step bunching of the 4H-SiC surface as well as preventing dopant out-diffusion. For each of the three sample sets, 1 μm of TEOS SiO_2 was used as the capping layer. This was selected due to the simplicity in depositing and removing the layer, in comparison with graphite (converted from photoresist) layers [171]. After the anneal process and subsequent cap removal in dilute HF solution, the passivation, metallisation and contact annealing processes as described in Section 7.3.1 have been carried out. However, this process was extended to include metal overlayers on both sides

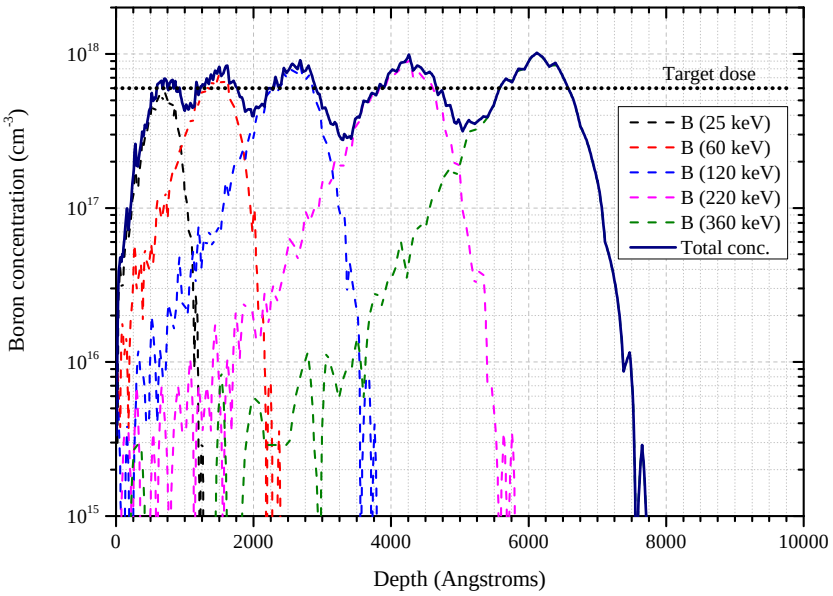


Figure 7.10: Simulated implanted box profile of medium-dose boron in 4H-SiC.

of the samples, to facilitate the mounting and wire bonding of the devices to direct copper bond (DCB) substrates. For the top (wire-bonded) side of the samples, a ∼1 μm thick Al layer was deposited; for the back (soldered) side, a ∼1 μm thick Ag layer was deposited.

7.4.2 Physical Characterisation Results

7.4.2.1 SIMS Analysis

In order to determine the profile of the implanted B, and how the profile is affected by different annealing conditions, dynamic SIMS has been employed. Figure 7.11 shows the experimental as-implanted medium-dose B profile compared to the SRIM simulated profile. It can be seen that the experimental profile is similar to the simulated profile, though with a higher surface concentration and a more gradual tail. This high surface

concentration was initially attributed to the fact that a thin (10 nm) layer of Au was deposited onto the 4H-SiC surface to minimise sample charging issues; the Au used was not ultra-pure and is expected to contain some boron. Contrary to this, Troffer et al. [172] suggests that a pile-up of B near the surface is due to the diffusion of the dopant in the semiconductor bulk. However, because this high B concentration is also evident in the SIMS profile for the as-implanted sample, it is reasonable to conclude that it is due to the layer of Au applied prior to the SIMS measurements. Moreover, the peak in concentration is within the first 10 nm of the SIMS depth profiles, which represent the Au layer. Though not shown here, the other two implant doses exhibited similar deviations from the corresponding simulated profiles.

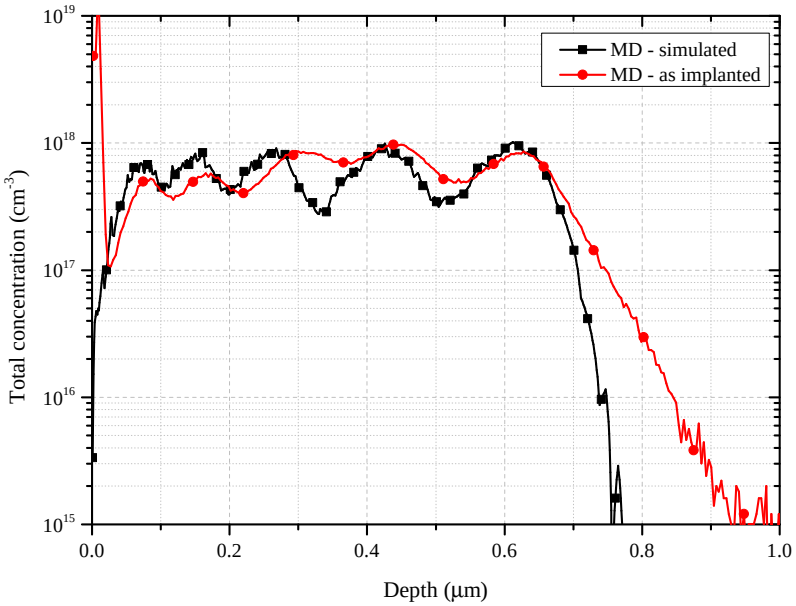


Figure 7.11: Experimental and simulated implanted box profile of medium-dose boron in 4H-SiC.

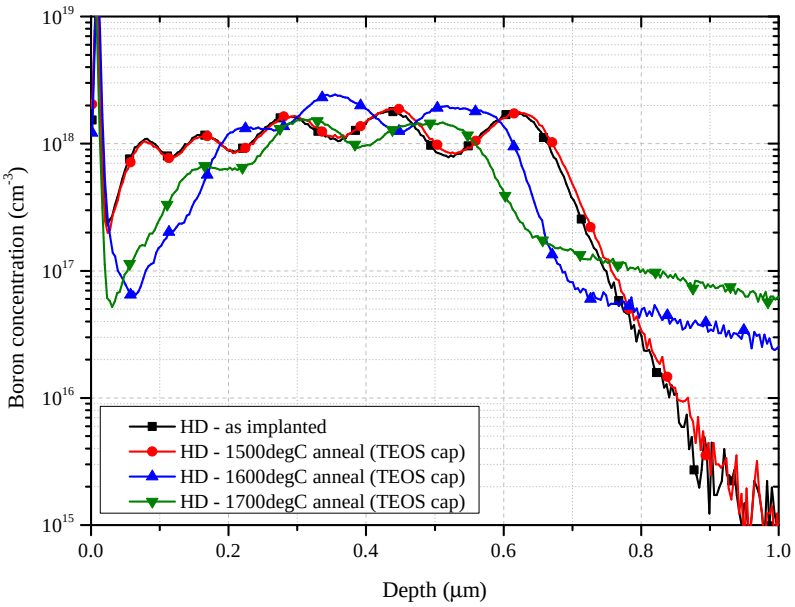


Figure 7.12: Experimental implanted box profile of high-dose boron in 4H-SiC for a range of annealing temperatures. All anneals were done with a TEOS SiO_2 capping layer.

Shown in Figure 7.12 are the implanted boron profiles after annealing at 1500°C, 1600°C and 1700°C (each for 30 minutes) compared against the as-implanted profile. It can be seen that the anneal at 1500°C has had very little effect on the B profile in the 4H-SiC, whilst the 1600°C and 1700°C anneals have both caused diffusion of the B into the bulk. As expected, this diffusion increases with increasing temperature [172]. There is also a notable drop in concentration close to the surface of the 4H-SiC for the samples annealed at 1600°C and 1700°C, suggesting that some out-diffusion of B has occurred, despite the use of a TEOS SiO_2 capping layer. It can also be inferred from Figure 7.12 that although a capping layer was used, and the anneal was performed in an Ar ambient, the 4H-SiC surface was being unintentionally thermally oxidised during the process. This

is evident from the increasing shift in the implanted B profiles towards the surface with increasing anneal temperature, which represents the amount of 4H-SiC consumed during the annealing processes.

Figure 7.13 shows the implanted boron profiles annealed at 1700°C with and without the TEOS SiO_2 capping layer. It can be seen from the increased shift in the implanted B profile towards the 4H-SiC surface that a greater amount of the 4H-SiC was consumed in the sample without the TEOS capping layer, due to the unintentional thermal oxidation that occurred during the anneal process. However, upon evaluation of these SIMS results, some of the findings were not as expected. It can be seen from Figure 7.13 that the B concentration near the 4H-SiC surface of the sample annealed at 1700°C without the TEOS capping layer does not show the same dip in concentration as the samples annealed with the TEOS cap. Because the annealing process has introduced thermal oxidation of the 4H-SiC, it was expected that any sample without a capping layer would oxidise more readily as well as being more susceptible to dopant out-diffusion. Though the non-capped sample has oxidised to a greater extent, the dopant out-diffusion appears significantly less severe. In addition, by integrating to determine the area underneath the depth profile of each of the samples, it was found that the sample annealed at 1700°C without the TEOS cap had a higher quantity of residual B atoms when compared against the sample annealed with the TEOS cap.

These results suggest that the TEOS capping layer is ineffective in preventing the out-diffusion of implanted B during activation anneal processes at 1600°C and over, and thus is not suitable for use in these processes. However, across all annealed samples, the volume of B atoms remaining was higher than for similar annealing experiments previously reported [141, 172]. The out-diffusion that occurs in B-implanted 4H-SiC is attributed to the kick-out mechanism [173], which is also the process for B diffusion in Si. The kick-out

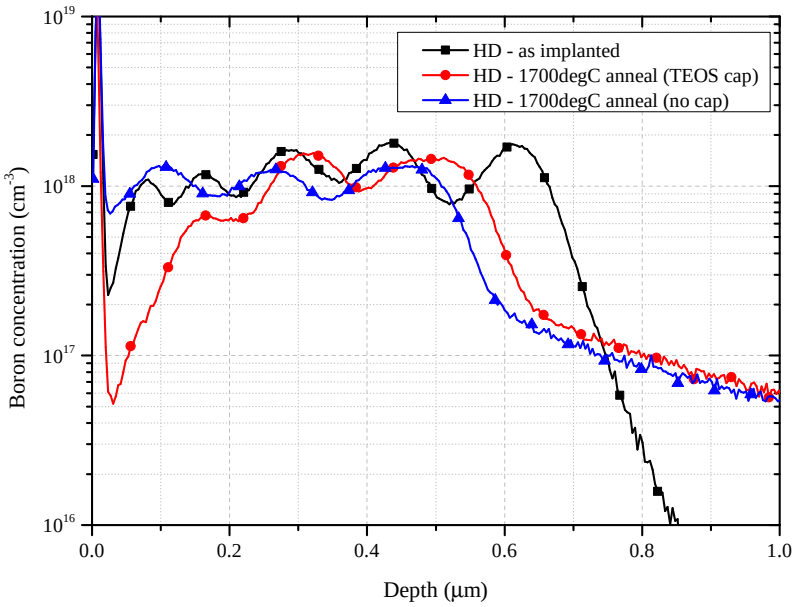


Figure 7.13: Experimental implanted box profiles of high-dose boron in 4H-SiC annealed at 1700°C with and without TEOS SiO_2 capping layer.

mechanism describes B diffusion to begin when a free interstitial Si atom encounters a substitutional B atom and exchanges with it, thus leaving an interstitial B atom in the crystal lattice. The B atom then travels rapidly in the interstices until it exchanges with another Si atom in the lattice, therefore becoming substitutional again and regenerating an interstitial Si atom.

In [141], it is suggested that co-implantation of C atoms can suppress the B out-diffusion by reducing the supersaturation of interstitial Si atoms. The high concentration of C atoms has been proposed to either form complexes with the interstitial Si atoms, or to diffuse (also via the kick-out mechanism) and cause an undersaturation of interstitial Si atoms. Further evidence of the dependence of B out-diffusion on interstitial Si atoms was presented in [174], in which accurate modelling based on the kick-out diffusion mechanism

of experimental implanted B profiles was achieved, leading the authors to confirm that interstitial Si atoms, rather than Si vacancies, were the cause of B out-diffusion. Since the thermal oxidation of 4H-SiC results in a supply of excess C atoms in the semiconductor bulk, this explains the diffusion characteristics of the B implanted annealed samples that have been presented in this Section.

7.4.2.2 Raman Spectroscopy Analysis

For the JTE-implanted PiN diodes, the use of Raman spectroscopy for analysing the effectiveness of post-implant annealing processes on the crystal recovery is of significant interest. As outlined in [153], the LO phonon region of the Raman spectra is expected to consist of a broad and shallow peak in an as-implanted sample, which indicates amorphisation of the 4H-SiC crystal, and a sharp peak in unprocessed crystalline 4H-SiC. For an increasing anneal temperature of implanted material, the LO phonon peak is expected to shift to a higher frequency and broaden asymmetrically; this illustrates an increase in the free carrier density. For lower annealing temperatures ($\leq$1400°C for phosphorous (P) implanted 4H-SiC), sharp LO phonon peaks were observed in [153]; these were attributed to an incomplete recovery in crystallinity that generated a large number of deep level defects acting as traps for free carriers.

The Raman spectra of the annealed high-dose B-implanted samples alongside the control (unprocessed) 4H-SiC sample and the as-implanted sample is shown in Figure 7.14. Shown inset in the Figure is the LO phonon region of the spectra. As expected, the LO phonon peak in the as-implanted sample is the least intense spectra, suggesting some amorphization of the 4H-SiC material. In addition, the control sample spectra shows the

expected Raman profile. Using Lorentzian fitting parameters as described by

$$y = y_0 + \frac{2A}{\pi}\frac{w}{4(x - x_c)^2 + w^2} \tag{7.11}$$

where the parameters are as illustrated in Figure 7.15, the LO band of the control sample peaks at 967.5 cm^{-1} and the as-implanted sample peaks at 965.4 cm^{-1}. This is in contrast to the respective values of 964.1 cm^{-1} and 956.1 cm^{-1} that were experimentally found in [153]. However, the fact that the Raman spectra for the as-implanted high-dose B sample shows less of a shift towards a lower frequency than the results for the P implanted (to a concentration of 3.0×10^{18} cm^{-3}) sample in [153] suggests that the 4H-SiC crystal hasn't been amorphised to the same extent; this is due to the lower relative atomic mass of B compared to P (10.81 for B and 30.97 for P) and the lower implanted doping concentration used (8.0×10^{17} cm^{-3} for the B implantation and 3.0×10^{18} cm^{-3} for the P implantation).

Looking at the Raman spectra for the annealed samples, it can be seen that there are relatively small differences between the measurements, though they all show departures from the control sample and the as-implanted sample spectra. However, after performing a Lorentzian fit of the data, it has been found that the LO phonon peak shifts towards a higher frequency in proportion to the annealing temperature, which was also reported in [153]. However, it is noted that the shift in frequency is relatively modest, from 966 cm^{-1} for the sample annealed at 1500°C to 968 cm^{-1} for the sample annealed at 1700°C.

By analysing the Raman data alongside the SIMS data presented in Section 7.4.2.1, the fact that the data for the annealed samples doesn't fully show the expected trend can be explained. As outlined in [153], the penetration depth of the 244 nm wavelength

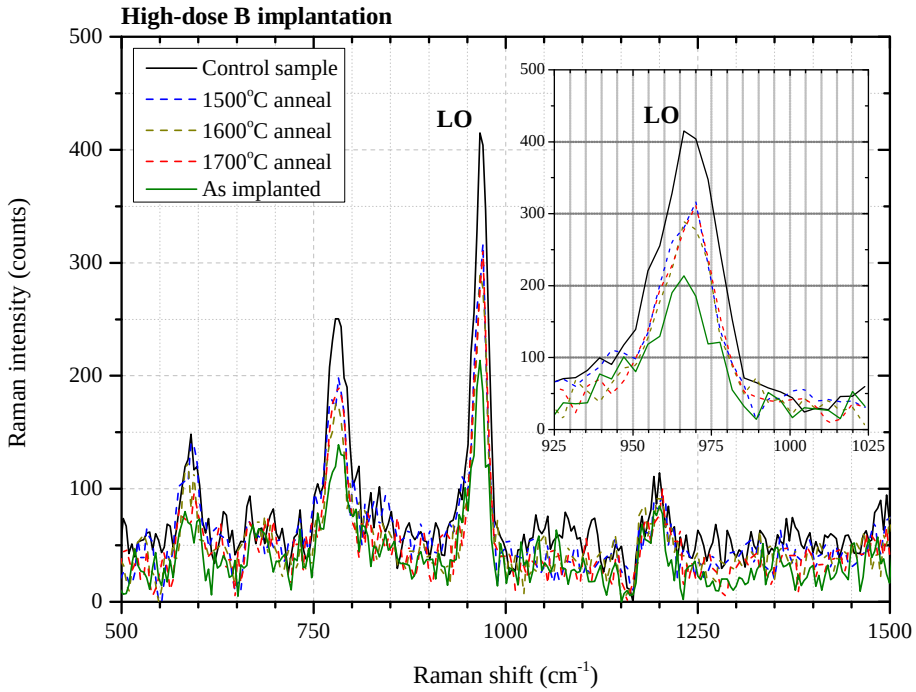


Figure 7.14: Raman spectra of high-dose B-implanted samples. The spectra for the unprocessed control sample is also shown, for comparison.

laser used in this work is around 50-100 nm. For the implanted box profile described in Section 7.4.1, the use of this laser wavelength is ideal for Raman analysis, and the Raman spectra for the both the unimplanted and the as-implanted samples were in line with expectations. In addition, the sample annealed at 1500°C peaks at a similar frequency to the as-implanted sample, and has a sharper peak (lower w), which suggests that the 1500°C anneal for B-implanted 4H-SIC is insufficient for recovering crystallinity in the 4H-SiC. The SIMS data correlates with this, as only a negligible difference was observed between the as-implanted and the 1500°C annealed samples. However, it is evident from the SIMS data for the 1600°C and 1700°C annealed samples that diffusion of the implanted B has had a significant impact on the doping profile in the 4H-SiC within 100 nm of the

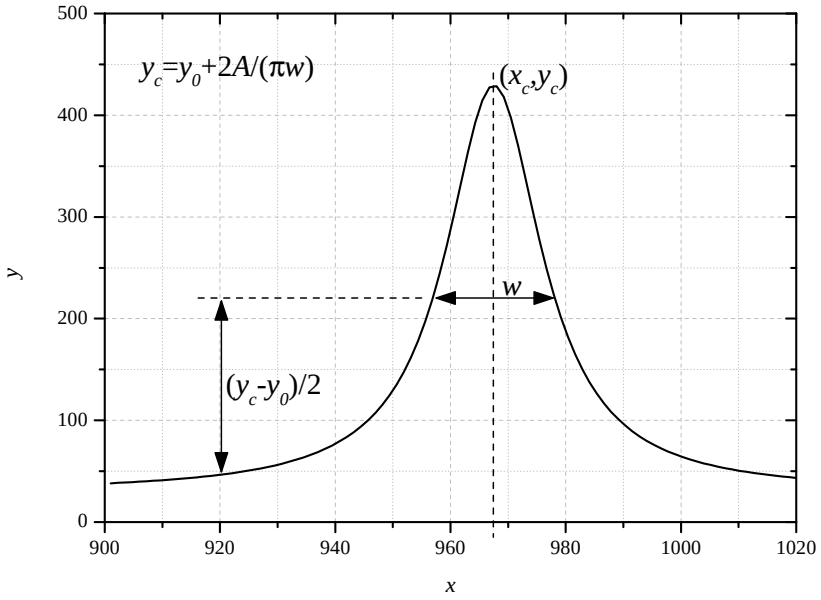


Figure 7.15: Lorentzian fitting parameters for Raman spectra.

surface, with a much lower concentration of B being present than intended. As such, this explains why the Raman spectra for these two samples did not show the expected trend in relation to the other samples.

7.4.2.3 AFM Analysis

As discussed in Section 3.4.2, the use of high temperature implant activation annealing processes can cause roughening of the 4H-SiC surface. From a device performance viewpoint this is of great concern, as a poor surface morphology will result in enhanced surface recombination, thus potentially degrading both forward and reverse device characteristics. The use of a capping layer during the annealing process is intended to prevent the surface roughening, with graphite converted from photoresist being the typical material

employed [110]. As outlined previously in this Chapter, a TEOS SiO_2 capping layer was used when performing the implant anneal for the second generation 3.3 kV PiN diodes. Though the SIMS analysis indicated that the TEOS cap wasn't able to prevent out-diffusion of implanted B during the high temperature anneal processes, AFM has been employed to investigate the ability of TEOS SiO_2 to protect the 4H-SiC surface during the annealing processes. All AFM imaging and analysis presented in this Section has been performed using the Gwyddion software package [175].

In order to provide a benchmark for the AFM analysis of the annealed samples, the surface morphology of a 4H-SiC control sample having undergone no implantation or annealing has been characterised; this is shown in Figure 7.16. Based on a 1 μm scan size, the rms surface roughness was measured to be 0.277 nm. It can seen from this Figure that the striped surface morphology indicative of atomic steps is present.

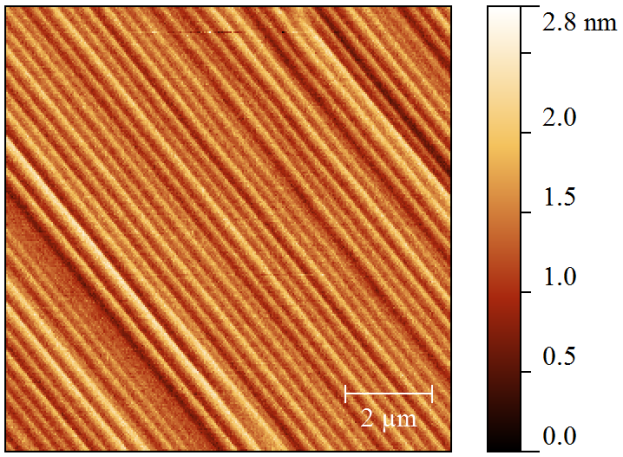
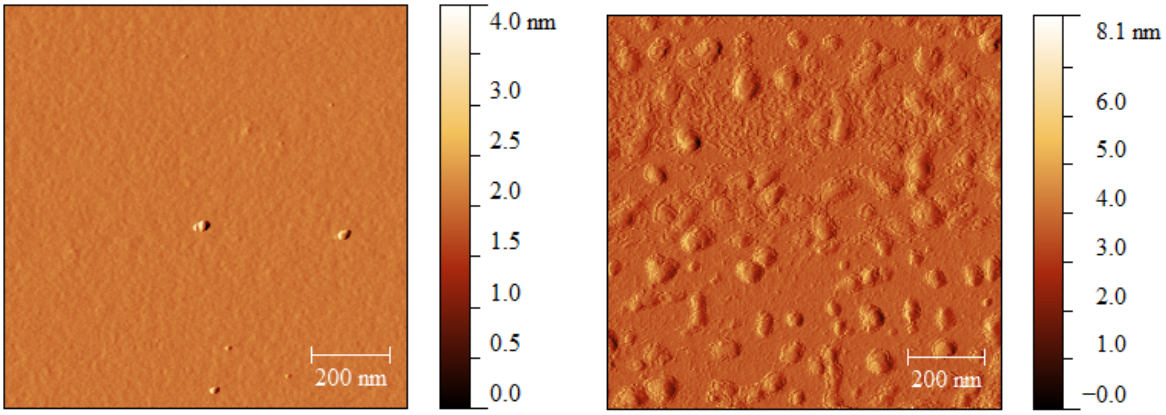


Figure 7.16: AFM scan of unannealed 4H-SiC control sample.

Figure 7.17 shows the AFM scans for the B-implanted samples annealed at 1500°C, both with and without the TEOS SiO_2 capping layer (both scans were performed after a HF etch to remove any SiO_2 present). It is evident that the sample annealed with the

TEOS SiO_2 cap has a considerably worse surface morphology, suggesting that the SiO_2 could not be fully removed from the 4H-SiC surface in dilute HF solution, possibly due to the amorphous SiO_2 being converted to a crystalline phase [176]. The rms surface roughness of the TEOS-capped sample was measured to be 0.526 nm, this compares to 0.081 nm for the uncapped sample.

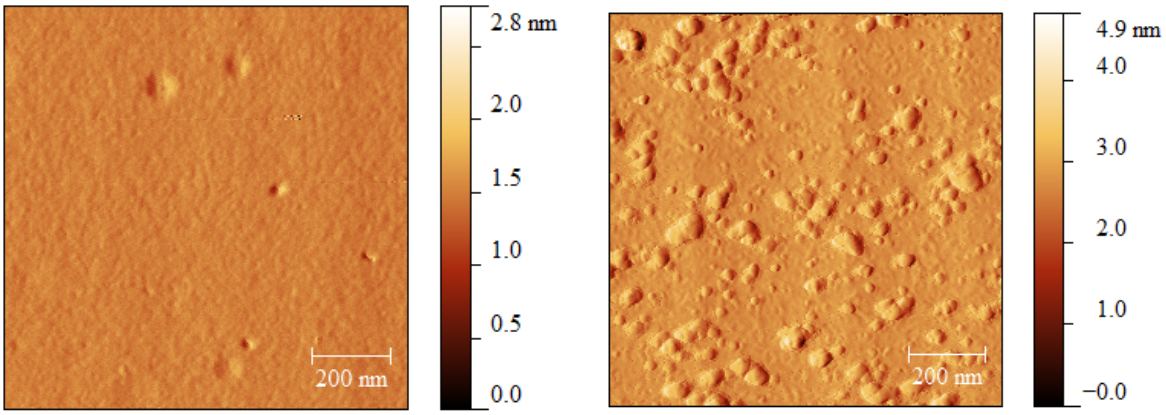


(a) (b)

Figure 7.17: AFM scans of B-implanted 4H-SiC samples annealed at 1500°C. (a) shows the sample annealed without a capping layer and (b) shows the sample annealed with a TEOS SiO_2 capping layer. The three distinct features in (a) are suspected to be particles on the 4H-SiC surface (as AFM was performed outside the cleanroom environment).

Both the 1600°C (shown in Figure 7.18) and 1700°C (shown in Figure 7.19) TEOS-capped annealed samples show a similar surface morphology to the sample annealed at 1500°C, with rms surface roughness values of 0.353 nm and 0.406 nm respectively. In addition, the sample annealed at 1600°C without the TEOS capping layer had a surface morphology similar to the 1500°C annealed sample, with a rms surface roughness of 0.075 nm. However, the surface morphology of the sample annealed at 1700°C without the TEOS cap was considerably worse than the other two samples, with a rms surface roughness of 0.378 nm. Across all three annealing temperatures, it is evident that no step

bunching has occurred during the activation anneal processes; this is attributed to the fact that in each case the 4H-SiC surfaces have thermally oxidised during the process, as opposed to being protected by a resilient capping layer. As such, the morphology of the surfaces of the uncapped samples are indicative of those that would be achieved during thermal oxidation processes. It can therefore be seen that performing thermal oxidation at 1700°C is detrimental to the quality of the 4H-SiC/SiO_2 interface, and would thus be expected to yield relatively poor quality device characteristics.

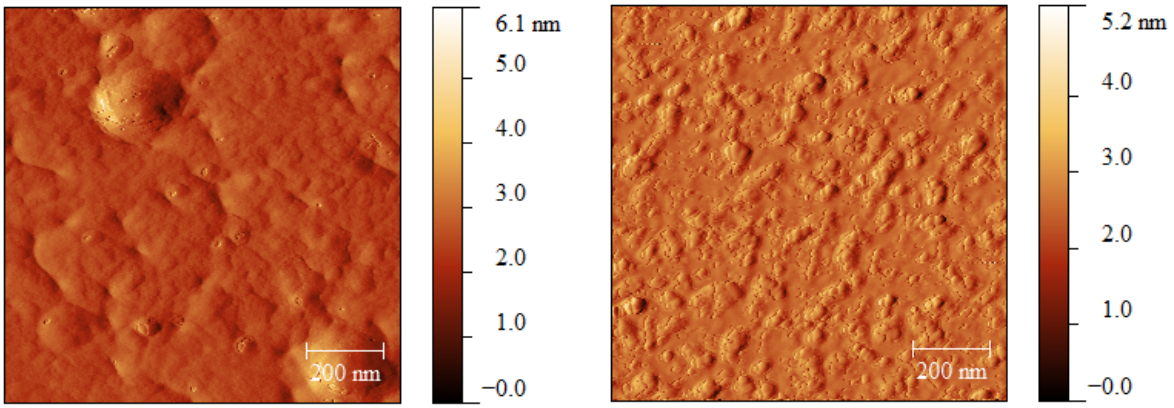


(a) (b)

Figure 7.18: AFM scans of B-implanted 4H-SiC samples annealed at 1600°C. (a) shows the sample annealed without a capping layer and (b) shows the sample annealed with a TEOS SiO_2 capping layer.

7.4.3 Reverse I-V Characterisation Results

Figures 7.20, 7.21 and 7.22 show the reverse log(J)-V characteristics (up to 100 V reverse bias) for the PiN diodes with low-dose, medium-dose and high-dose JTE structures respectively. It can be seen that, overall, the second generation 3.3 kV PiN diodes typically exhibit lower reverse leakage currents (at 100 V reverse bias) than the first generation devices (shown in Figure 7.6). The reverse leakage current results for the PiN



(a) (b)

Figure 7.19: AFM scans of B-implanted 4H-SiC samples annealed at 1700°C. (a) shows the sample annealed without a capping layer and (b) shows the sample annealed with a TEOS SiO_2 capping layer.

diodes annealed at 1700°C, which, excluding the devices suspected of containing defects compromising their reverse characteristics, range between around 100 pA/cm^2 to over 10 mA/cm^2. This significant variation in performance is attributed to the large amount of B diffusion within the semiconductor that occurred during the anneal process.

A summary of the complete set of data (excluding devices suspected of containing micropipes) for the reverse leakage currents of the second generation 3.3 kV PiN diodes is given in Figure 7.23. In this Figure, the geometric mean and standard deviation have been plotted for each of the JTE doses and annealing temperatures. It can be seen that the medium (optimum) JTE dose has the lowest reverse leakage current across the range of annealing temperatures, with the devices annealed at 1600°C typically exhibiting the best characteristics. It is also evident that the data for the PiN diodes with the high-dose JTE do not follow the same trend as the low- and medium-dose JTE devices; from observation of Figure 7.22 it can seen that two of the devices annealed at 1600°C, one small- and one large-area from the same side of the die, have uncharacteristically poor

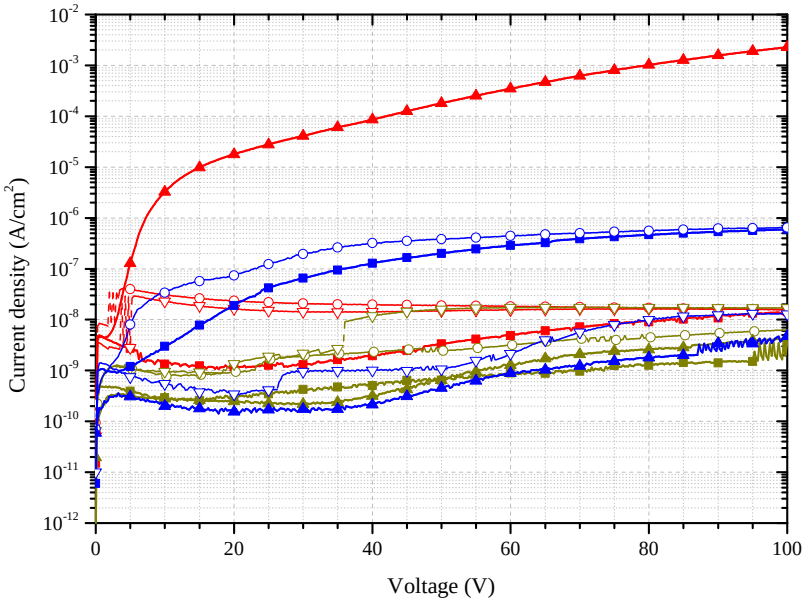


Figure 7.20: Reverse log(J)-V characteristics of second generation 3.3 kV 4H-SiC PiN diodes with low dose JTE implant at 25°C. Anneal temperatures of 1500°C, 1600°C and 1700°C are represented by blue, dark yellow and red traces respectively. Large-area device characteristics have solid markers and lines, whilst small-area device characteristics have open markers and dashed lines.

reverse leakage current characteristics. Visual inspection of the die suggested that these two devices have been fabricated on material that is at least partially within the exclusion zone at the periphery of the wafer, which explains the poor characteristics that have been observed.

The reverse breakdown characteristics of the second generation 3.3 kV PiN diodes are shown in Figure 7.24. These characteristics were obtained using the Tektronix 371B high power curve tracer (3 kV output capability). There are 9 sub-plots in this Figure; data for each of the three implant doses and anneal temperatures is shown. Each sub-plot was intended to contain 4 reverse breakdown characteristics; unfortunately some

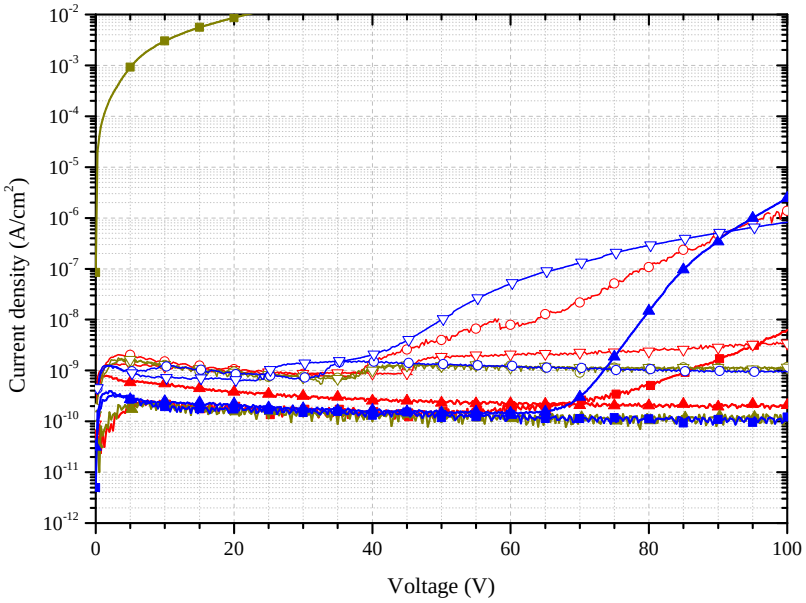


Figure 7.21: Reverse log(J)-V characteristics of second generation 3.3 kV 4H-SiC PiN diodes with medium dose JTE implant at 25°C. Anneal temperatures of 1500°C, 1600°C and 1700°C are represented by blue, dark yellow and red traces respectively. Large-area device characteristics have solid markers and lines, whilst small-area device characteristics have open markers and dashed lines.

devices were damaged during testing and as such some of the sub-plots do not contain all 4 device characteristics. Though not shown in this Figure, the maximum reverse breakdown voltage achieved on un-terminated 3.3 kV PiN diodes was 390 V at 1 mA reverse current. It is evident that, regardless of JTE implant dose, the samples annealed at 1500°C showed consistently low breakdown voltages of approximately 600 V at 1 mA, illustrating that there was insufficient activation of the implanted B atoms, even when performing the ion implantation process at 650°C.

In line with the numerical simulation results presented in Chapter 4, the PiN diodes with the medium-dose (1.5×10^{17} cm^{-3}) JTE showed the best reverse breakdown perfor-

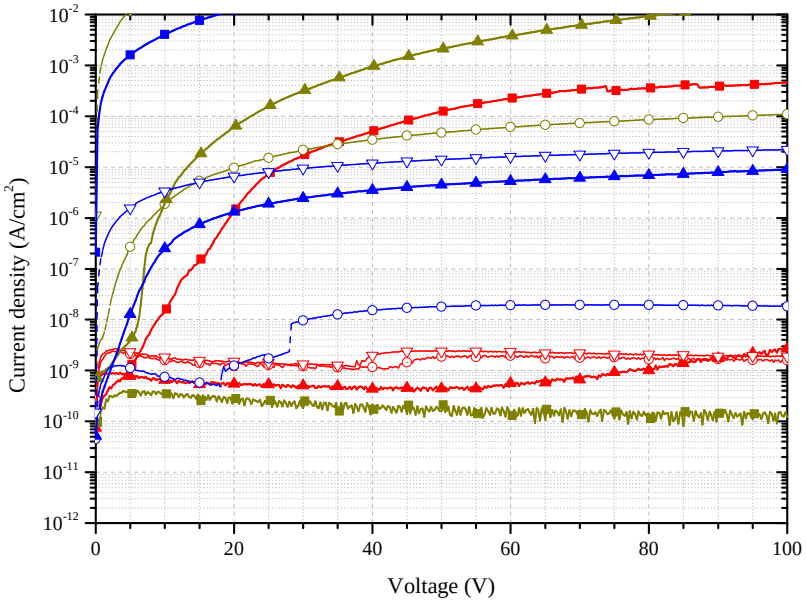


Figure 7.22: Reverse log(J)-V characteristics of second generation 3.3 kV 4H-SiC PiN diodes with high dose JTE implant at 25°C. Anneal temperatures of 1500°C, 1600°C and 1700°C are represented by blue, dark yellow and red traces respectively. Large-area device characteristics have solid markers and lines, whilst small-area device characteristics have open markers and dashed lines.

mance, with a small-area device annealed at 1600°C found to have the maximum achieved breakdown voltage of 2.8 kV at 1 mA, which equated to around 85% of the targeted value of 3.3 kV. The results for the PiN diodes that underwent an anneal at 1700°C exhibited a greater spread in the achieved breakdown voltage of individual devices; this is attributed to the increased diffusion of the implanted B at this temperature, resulting in a doping profile within the semiconductor that departed significantly from the intended profile. The reverse breakdown performance of all of the second generation 3.3 kV PiN diodes with edge termination is summarised in Figure 7.25.

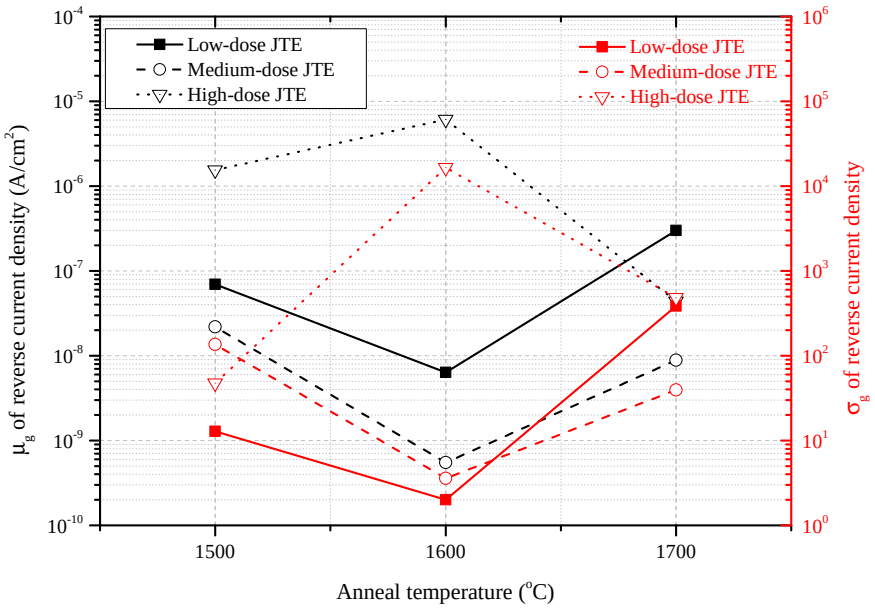


Figure 7.23: Geometric mean and standard deviation of reverse current density as a function of annealing temperature of second generation 3.3 kV 4H-SiC PiN diodes at 25°C.

7.5 Summary

In this Chapter, the fabrication and characterisation of 3.3 kV 4H-SiC PiN diodes has been presented. After outlining details of the photomask design and the epitaxial structures of the diodes fabricated in this Chapter, the PiN diode fabrication processes and characterisation results were presented. The small-area first generation PiN diodes, with an active area of 0.0011 cm^2, were measured to have a voltage drop of 4.8 V and a differential on-resistance of 17 $m\Omega$-cm^2 at 100 A/cm^2 and 25°C, and exhibited near-ideal forward characteristics. From the measured reverse saturation current, the carrier lifetime of the fabricated PiN diodes was estimated to be 480 ns. The reverse leakage currents of the first generation devices were found to vary significantly, from approximately 5 nA/cm^2 to

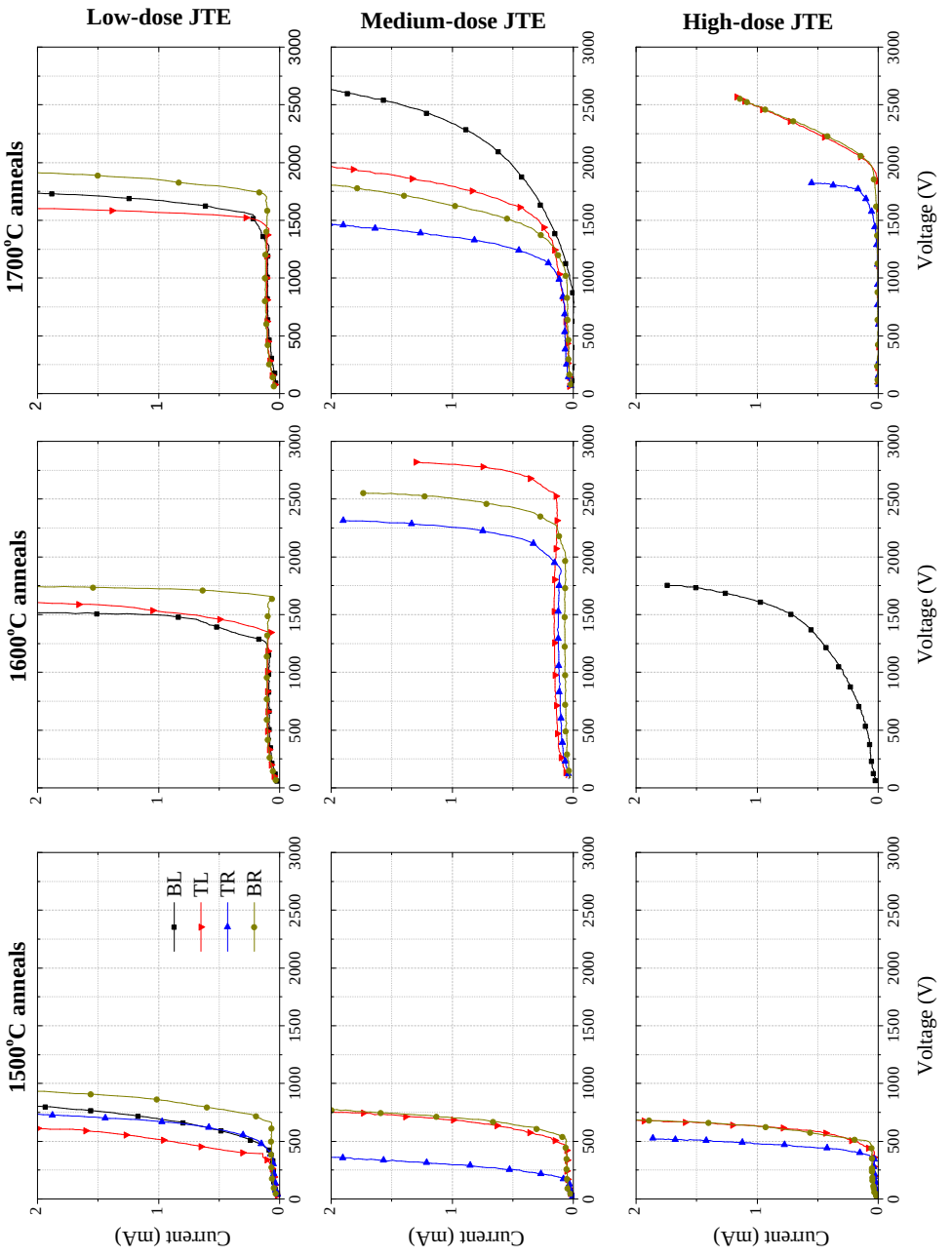


Figure 7.24: Reverse breakdown characteristics of second generation 3.3 kV 4H-SiC PiN diodes.

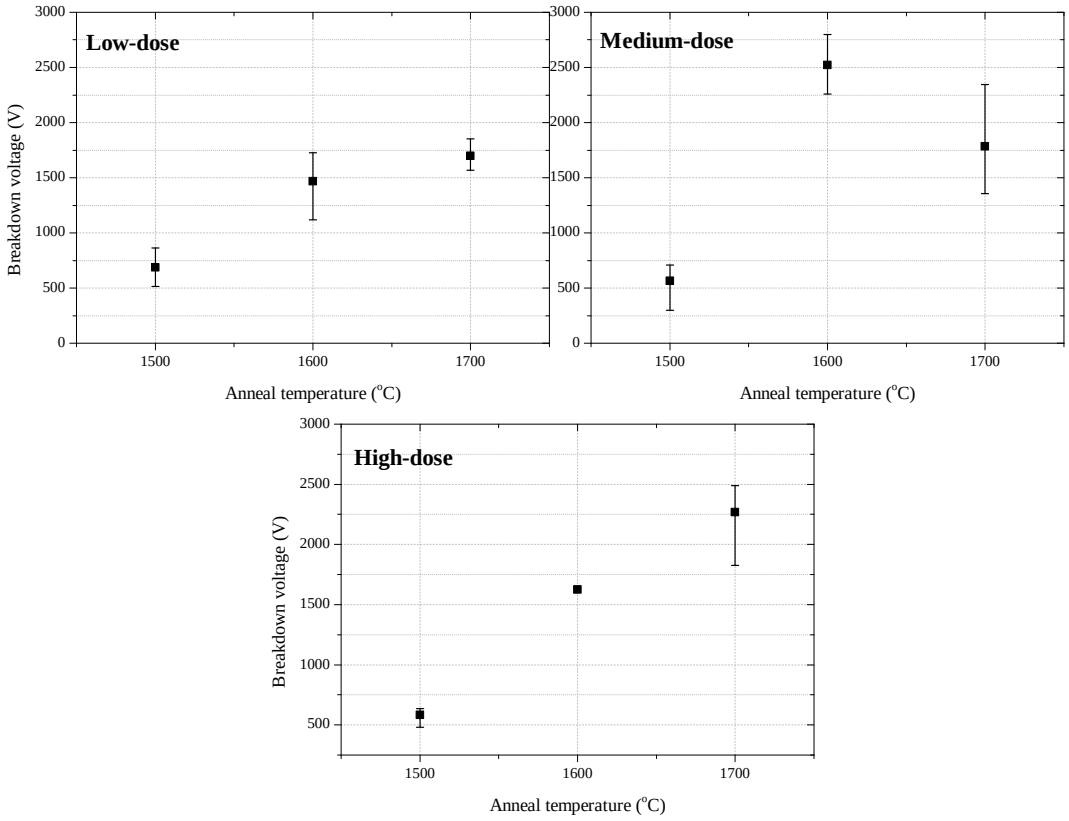


Figure 7.25: Reverse breakdown voltage as a function of annealing temperature of second generation 3.3 kV 4H-SiC PiN diodes at 25°C. Each statistical data point refers to a maximum of 4 devices.

200 μA/cm^2 at 100 V and 25°C, excluding devices suspected of containing micro pipes.

The fabrication of the first generation of 3.3 kV PiN diodes highlighted a device performance problem when a metal overlayer was used, in that under low-level injection conditions the J-V characteristics were no longer dominated by recombination-generation, i.e. exhibiting an ideality factor of $\eta = 2$. This was concluded to be due to an insufficient thickness of the passivation oxide, which meant that a current path parallel to the diode *pn* was present. A simple modification to the passivation process was suggested, which would prevent this occurring in future generations of PiN diodes.

The second generation of 3.3 kV PiN diodes added the B-implanted SM-JTE edge termination designed in Chapter 4 to the device structure, with the aim of blocking the targeted 3.3 kV. A range of implant dose and anneal temperatures were investigated, and the implanted devices were characterised physically, to determine the effect of annealing on the surface morphology of the 4H-SiC as well as the doping profiles within the semiconductor, and electrically, to determine the reverse breakdown voltage of the PiN diodes. SIMS analysis showed that an annealing temperature of 1500°C was insufficient to displace the implanted B atoms from their as-implanted locations, though the B atoms diffused at 1600°C and to a greater extent at 1700°C. The SIMS analysis also showed that the TEOS SiO_2 was unsuitable for use as a capping layer, as out-diffusion of B atoms was observed at annealing temperatures down to 1600°C. AFM analysis also highlighted a problem with the use of TEOS SiO_2 as a capping layer across the entire range of anneal temperatures, as all samples annealed with the TEOS cap exhibited worse surface morphology than the samples annealed without the capping layer.

The electrical characterisation of the second generation 3.3 kV PiN diodes showed that the best performing devices had an B implantation dose of 2.0×10^{13} cm^{-2} and were annealed at 1600°C, with the maximum achieved reverse breakdown voltage being 2.8 kV,

which was approximately 85% of the targeted breakdown voltage of 3.3 kV. Devices annealed at 1500°C all exhibited relatively low reverse breakdown voltages, regardless of implantation dose, highlighting that this anneal temperature is insufficient for activation B dopant atoms in 4H-SiC. Devices annealed at 1700°C showed reverse breakdown characteristics similar to those annealed at 1600°C though with greater variance; this was attributed to the increased diffusion of the implanted B atoms at 1700°C.

Chapter

8 Fabrication and Characterisation of 10 kV 4H-SiC PiN Diodes

Following the fabrication and characterisation of 3.3 kV-rated 4H-SiC PiN diodes, devices designed for a blocking voltage of 10 kV are presented in this Chapter. As with Chapter 7, the discussion in this Chapter follows the chronological evolution of these devices. Firstly, the device epitaxial structures and details of the defect distribution in the 4H-SiC wafer used for the devices in this Chapter are presented. The discussion then proceeds to the first generation of 10 kV PiN diodes, in which the impact of high temperature thermal oxidation processes were investigated on the electrical characteristics of fabricated PiN diodes. Following this, second generation 10 kV PiN diodes are presented; a novel combined high temperature thermal oxidation / annealing process was applied to these devices with the aim of further improving their characteristics, both forward I-V and clamped inductive switching characterisation has been used to analyse the static and transient performance of these PiN diodes.

8.1 Device Structure

For the devices discussed in this Chapter, both the starting material and the epitaxy has been obtained from Norstel [32]. As before, a micropipe density of less than 1 per cm^2 was specified, and the epitaxial layers were grown in a continuous growth run in an Aixtron VP-508 single-wafer reactor. The epitaxial structure that was specified is illustrated in Figure 8.1. Again, the epiwafer has been laser-cut into 14×14 mm chips for subsequent processing; the defect map and the location of individual wafer chips subsequently referred to in this Chapter is shown in Figure 8.2.

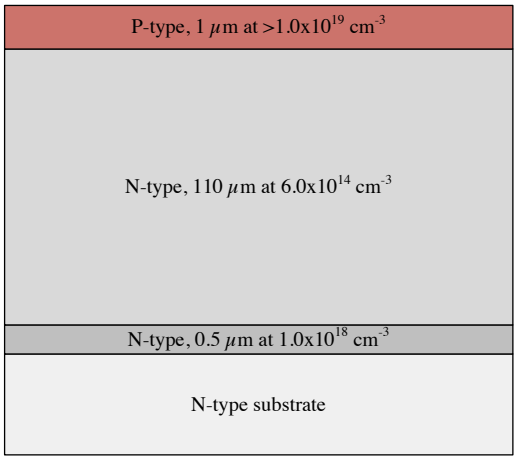


Figure 8.1: Epitaxial structure of 10 kV 4H-SiC PiN diodes.

8.2 First Generation 10 kV 4H-SiC PiN Diodes

As with the first generation of 3.3 kV PiN diodes, the devices presented in this Section have also been fabricated without edge termination, as it is the forward characteristics of the devices that are of principle interest. Four separate dies have been processed in this generation of devices, in order to investigate the use of high temperature thermal

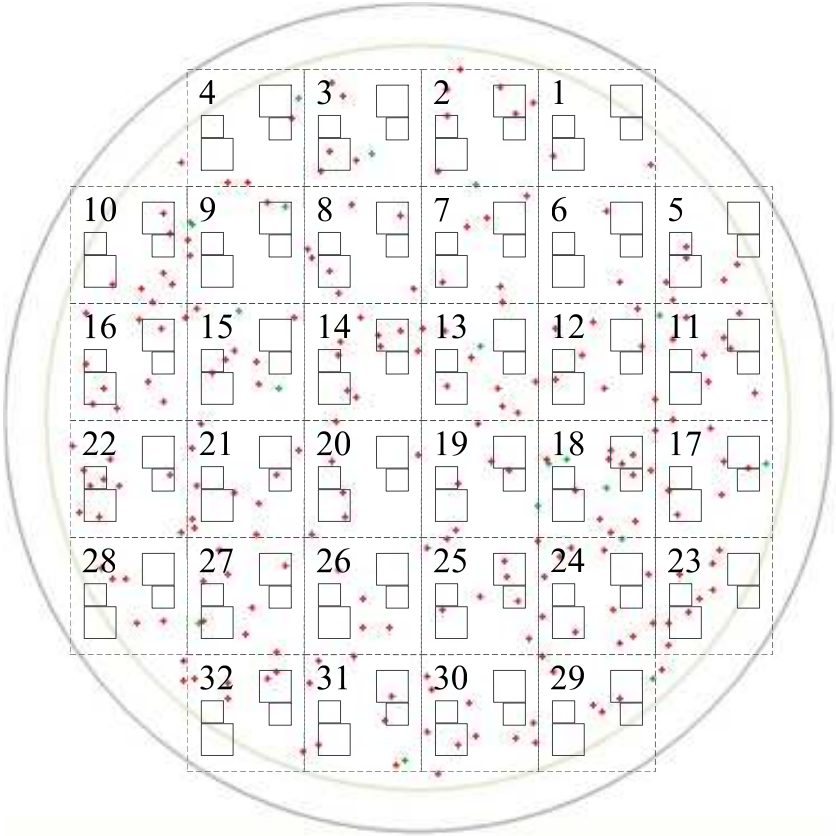


Figure 8.2: Defect map for 10 kV 4H-SiC epitaxial wafer supplied from Norstel. Red dots indicate triangle defects, green dots indicate downfall defects. A 3 mm exclusion zone is included at the wafer periphery. The locations of individual dies and the PiN diode areas on these dies have also been shown, along with their IDs.

oxidation for increasing the carrier lifetime and thus improving the forward characteristics of the PiN diodes. Each die has two different sized devices: a small-area diode with an active area of 0.006 cm^2, and a large-area diode with an active area of 0.031 cm^2 (DIE7 region on photomask). In addition to a control sample (die number 20 on Figure 8.2), the remaining three samples were oxidised at 1400°C, 1500°C and 1600°C (die numbers 6, 14 and 4 respectively). After device fabrication, the forward and (low-bias) reverse I-V characteristics of the diodes have been evaluated.

8.2.1 The Advantages of High Temperature Oxidation

It was first suggested in [177] that by performing thermal oxidation processes at temperatures higher than the conventional temperature of 1150°C (which is the typical limit of a quartz tube furnace), a better quality SiO_2/4H-SiC interface could be obtained, due to the more efficient removal of carbon at the interface. Moreover, the oxide growth rate is found to increase with increasing oxidation temperature [178]. In MOS-based devices, the better quality (low D_{it}) interface corresponds to a lower channel resistance, thus enabling better on-state performance. However, thermal oxidation studies in the literature are typically restricted to a maximum temperature of 1300°C or less, due to equipment limitations [4, 96, 177, 178].

As discussed in Chapter 3, the carrier lifetime in 4H-SiC has been found to be predominantly limited by the presence of the carbon vacancy-related $Z_{1/2}$ defect, and can be increased by generation of carbon interstitials that diffuse into the semiconductor bulk and effectively repair these defects. In the context of enhancing the carrier lifetime in 4H-SiC material by means of thermal oxidation, the increased oxidation rate and carbon removal at the SiO_2/4H-SiC interface at higher oxidation temperatures increases the rate at which the $Z_{1/2}$ defect is repaired in the semiconductor bulk, meaning that shorter oxidation times are required for repairing the defect in a given epitaxial layer thickness. In [179], it was shown that by increasing the oxidation temperature from 1300°C to 1400°C, the oxidation time could be reduced from 50 hours to 16.5 hours to eliminate the $Z_{1/2}$ defect to a depth of 100 μm. Though the benefits of performing the thermal oxidation at higher temperatures are evident, research into the use of oxidation temperatures above 1400°C remains largely unexplored. As such, the use of oxidation temperatures up to 1600°C for carrier lifetime enhancement are investigated in this Chapter.

8.2.2 Fabrication Process

Samples first underwent the standard cleaning process outlined in Appendix B, followed by a thermal oxidation process at 1400°C, 1500°C and 1600°C, each for five minutes. This relatively short duration was chosen because of concern that the oxidation rate at 1600°C and the subsequent consumption of the 4H-SiC would be high enough to consume all of the p-type anode epitaxial layer. The control sample did not undergo any thermal oxidation process. The thermally-grown SiO_2 was then removed in dilute HF solution, and the device mesas were defined using ICP etching. TEOS SiO_2 was deposited for passivation; this was then patterned so that the ohmic contacts to the p-type anode could be formed. A Ti/Al metal scheme was used for the anode contact, and Ti/NiV was used for the cathode contact. The samples were then annealed using the RTA furnace at 600°C for 2 minutes followed by 1000°C for 2 minutes, in Ar. Finally, a 1 μm thick Al metal overlayer was deposited on the anode side and patterned using an Al wet etch solution.

8.2.3 Forward I-V Characterisation Results

The forward I(J)-V characteristics of the first generation 10 kV PiN diodes have been evaluated across the temperature range 25°C to 300°C, and up to 1 A current. This equates to a maximum current density of 166 A/cm^2 for the small-area diodes, and 32 A/cm^2 for the large-area devices. Four-point probing was used to minimise additional resistance effects arising from the measurements, and devices were characterised using the pulsed power mode on the parameter analyser, to prevent device self-heating.

Figures 8.3 and 8.4 show the forward J-V characteristics of a selected small-area PiN diode from the control sample die having undergone no thermal oxidation. At 25°C, the on-state voltage drop of the device is 4.54 V at 100 A/cm^2. From these Figures it is

evident that as the operating temperature is increased, both the turn-on voltage and the forward voltage drop decrease, with the on-state voltage drop reducing by approximately 15% to 3.84 V at 300°C. This improvement in the forward characteristics of the PiN diode at higher temperatures is expected, as the dopant ionisation in the p-type anode is improved, the carrier lifetime in the drift region is increased, and the ohmic contact resistance is decreased. These three effects combine to overcome the reduced mobility at higher temperatures, resulting in improved conduction characteristics.

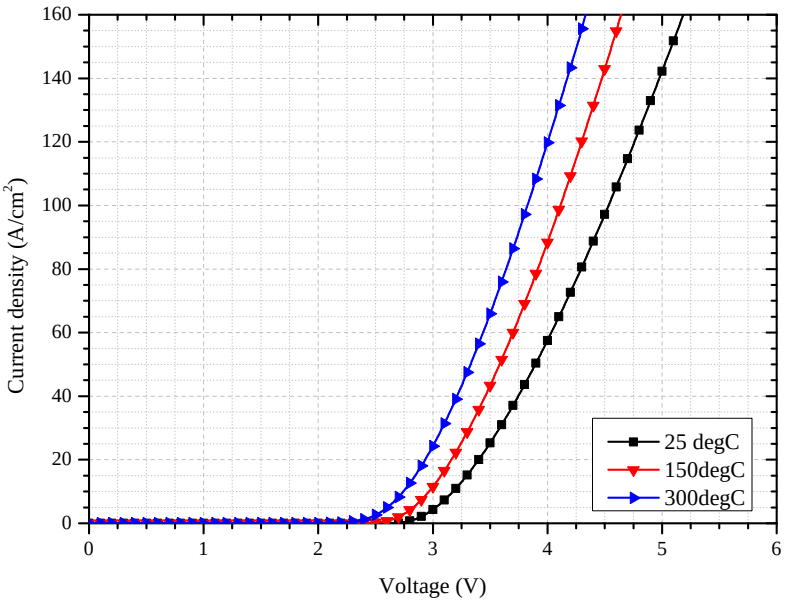


Figure 8.3: Forward J-V characteristics of small-area first generation control sample 10 kV PiN diode at 25°C, 150°C and 300°C.

Because the forward voltage drop of the control sample PiN diode is low when compared to the calculated voltage for an unmodulated PiN diode with identical drift region parameters, it is evident that the drift region contains a significant amount of modulating charge, thus reducing the on-state resistance of the device. In order to quantify the

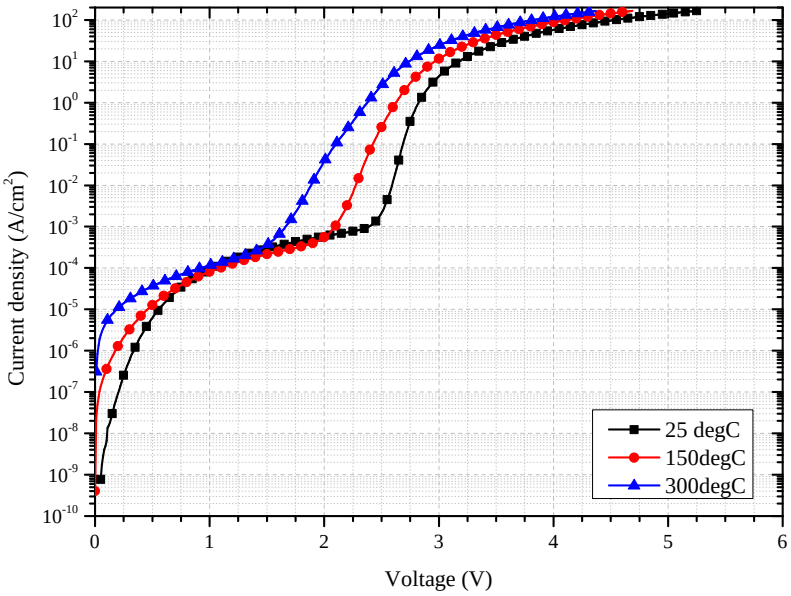


Figure 8.4: Forward log(J)-V characteristics of small-area first generation control sample 10 kV PiN diode at 25°C, 150°C and 300°C. The departures from the ideal J-V characteristic in the recombination current region are attributed to the presence of a parasitic Schottky diode in parallel with the *pn* junction.

magnitude of modulating charge that resides in the drift region under forward bias, the differential on-resistance of the PiN diode can be extracted using the expression introduced in Chapter 7, repeated here for ease

$$R_{on,diff} = \frac{dV(J_F)}{dJ_F} \tag{8.1}$$

Figure 8.5 shows the differential on-resistance as a function of current density of the control sample PiN diode at 25°C and 300°C. It can be seen that the resistance is large under low forward bias, due to the resistive drift region in the device, though as the forward bias increases, the conductivity modulation effect acts to reduce the resistance

in the drift region. At higher operating temperatures the initial resistance of the diode is increased due to the reduction in carrier mobility (shown more clearly in Figure 8.6), though at typical operating current densities, the improved dopant ionisation in the p-type anode, the longer carrier lifetime and the reduced contact resistance combine to lower the overall on-resistance of the device. For the small-area control sample, the differential on-resistance is approximately 11.6 mΩ-cm^2 at 100 A/cm^2 and 25°C, dropping to approximately 9.0 mΩ-cm^2 at 300°C. For the large-area control sample, the differential on-resistance is approximately 30.0 mΩ-cm^2 at 25 A/cm^2 and 25°C, dropping to approximately 19.5 mΩ-cm^2 at 300°C. In order to provide a direct comparison, the small-area diode has a differential on-resistance of approximately 18.1 mΩ-cm^2 at 25 A/cm^2 and 25°C, dropping to approximately 14.7 mΩ-cm^2 at 300°C.

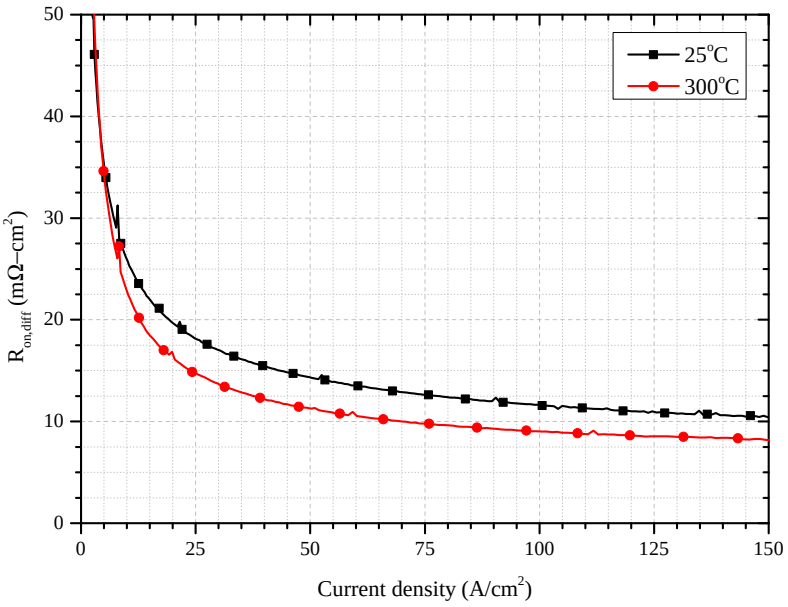


Figure 8.5: Differential on-resistance against current density of small-area first generation control sample 10 kV PiN diode at 25°C and 300°C.

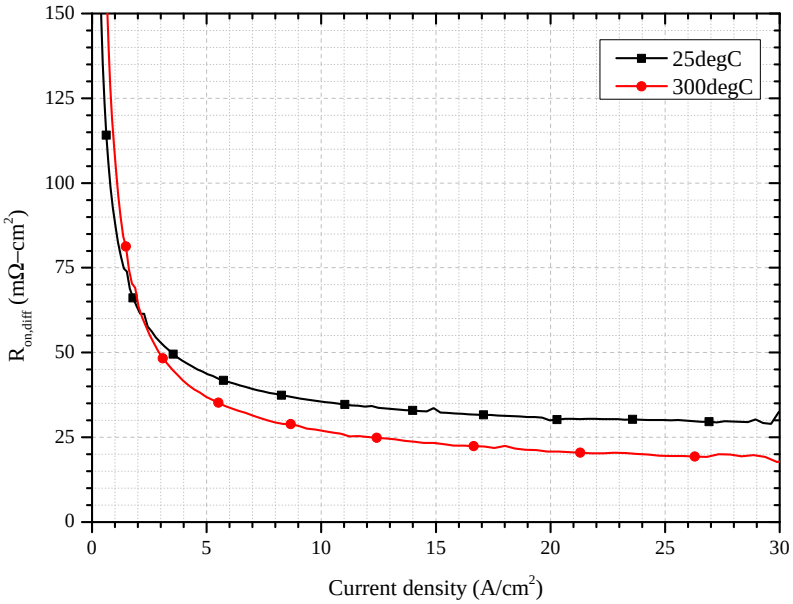


Figure 8.6: Differential on-resistance against current density of large-area first generation control sample 10 kV PiN diode at 25°C and 300°C.

Using the ideal diode equation introduced in Chapter 7, the ideality factor as a function of current density for the small-area control sample PiN diodes has been extracted; this characteristic is shown in Figures 8.7 respectively. It is evident that at low forward bias, the ideality factor is greater than the expected value of $\eta = 2$, indicating that current conduction mechanisms other than SRH recombination are active. This is attributed to the presence of unintentional current paths in parallel with the *pn* junction, as subsequent oxide thickness measurements indicated that the mesa etch depth was greater than the oxide thickness, meaning that the Al metal overlayer was in contact with the 4H-SiC surface. As the forward voltage bias approaches the built-in potential of the diode, it can be seen that, at 25°C, the ideality factor reaches a value of $\eta \approx 1.5$, which is higher than the expected value of $\eta = 1$. Based on the model proposed in [180] and previously

applied in Chapter 7, it can be assumed that there is one dominant shallow level and one dominant deep level that exist in the semiconductor, such that the ideality factor is $\eta = 3/2$. It is evident from these results that at even higher forward bias, the expected ideality factor of $\eta = 2$ in the high-level injection regime is not visible; this is attributed to the relatively high series resistance of the PiN diode.

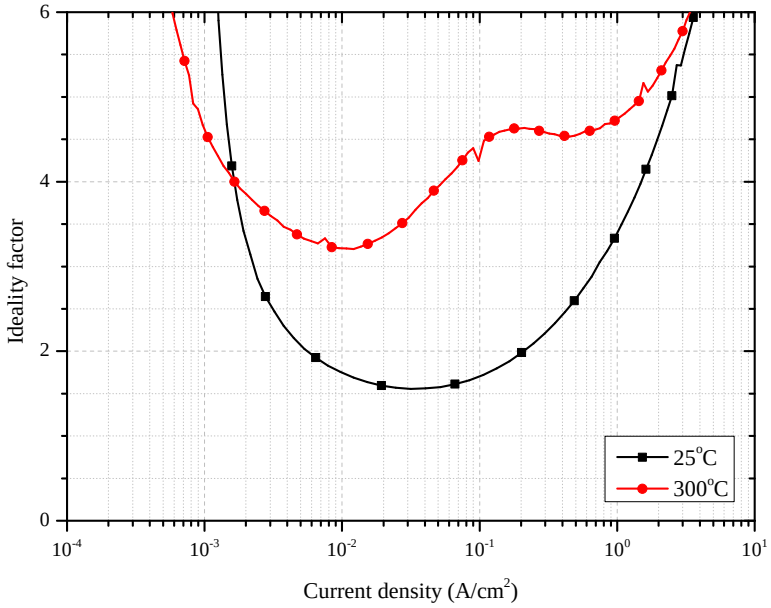


Figure 8.7: Ideality factor against current density of small-area first generation control sample 10 kV PiN diode at 25°C and 300°C.

Figure 8.8 shows the forward J-V characteristics of selected small-area thermally oxidised 10 kV PiN diodes compared to the characteristics of a control sample PiN diode. It is evident from this Figure that the forward characteristics of the diodes are improved after performing the thermal oxidation process, with the sample thermally oxidised at 1500°C demonstrating the best on-state performance when compared against the control sample and measured at 25°C. The complete set of forward J-V results for the first

generation 10 kV PiN diodes are summarised in Tables 8.1 and 8.2.

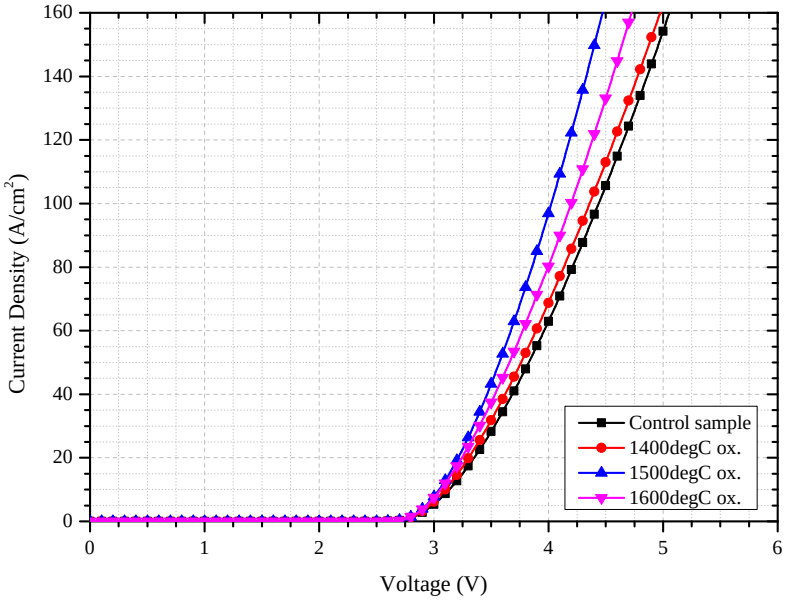


Figure 8.8: Forward J-V characteristics of thermally-oxidised small-area first generation 10 kV PiN diodes (measured at 50°C).

Table 8.1: Forward characteristics of small-area first generation 10 kV PiN diodes. All results presented correspond to a current density of 25 A/cm^2 (results in brackets correspond to 100 A/cm^2).

Diode ref.	V_F at 25°C (V)	$R_{on,diff}$ at 25°C (mΩ-cm^2)	V_F at 300°C (V)	$R_{on,diff}$ at 300°C (mΩ-cm^2)
PiN20-cont-S-A-1	3.50 (4.53)	18.1 (11.6)	3.01 (3.83)	14.7 (9.0)
PiN6-1400-S-A-1	3.47 (4.52)	17.8 (12.2)	2.87 (3.54)	12.1 (7.3)
PiN6-1400-S-A-2	3.60 (4.78)	17.5 (14.3)	2.88 (3.52)	11.9 (7.0)
PiN14-1500-S-A-1	3.35 (4.15)	14.2 (8.9)	2.86 (3.48)	11.3 (6.8)
PiN4-1600-S-A-1	3.43 (4.49)	18.5 (11.9)	2.77 (3.33)	10.1 (6.1)

Table 8.2: Forward characteristics of large-area first generation 10 kV PiN diodes. All results presented correspond to a current density of 25 A/cm^2.

Diode ref.	V_F at 25°C (V)	$R_{on,diff}$ at 25°C (mΩ-cm^2)	V_F at 300°C (V)	$R_{on,diff}$ at 300°C (mΩ-cm^2)
PiN20-cont-L-A-1	3.97	41.5	3.07	21.2
PiN20-cont-L-A-2	3.75	30.0	3.08	19.5
PiN6-1400-L-A-1	3.91	41.2	2.95	16.4
PiN14-1500-L-A-1	3.61	23.6	3.03	18.0
PiN4-1600-L-A-1	3.82	31.7	2.96	16.6
PiN4-1600-L-A-2	3.96	36.4	2.94	16.0

8.2.4 Reverse I-V Characterisation Results

The reverse J-V characteristics (up to 100 V reverse bias) of the first generation 10 kV PiN diodes are shown in Figure 8.9. It is evident that, aside from the devices that are suspected to contain micro pipes, the leakage currents are relatively high when compared against the 3.3 kV PiN diodes presented in Chapter 7. Furthermore, the characteristics of the small-area devices are generally worse than those of the large-area devices. This suggests that the leakage current is, at least partially, due to the mesa perimeter sidewall. This in turn suggests that the problem of a non-conformal passivation layer (previously discussed in Section 7.3.4) is still prevalent. To prevent this reoccurring, future generations of the 10 kV PiN diodes will need to employ a TEOS SiO_2 layer that is considerably thicker than the mesa etch depth.

8.3 Second Generation 10 kV 4H-SiC PiN Diodes

The results presented in Section 8.2 have illustrated that the use of high temperature thermal oxidation is beneficial in improving the on-state I(J)-V characteristics of the 4H-SiC high voltage PiN diodes. As such, a novel combined thermal oxidation and annealing

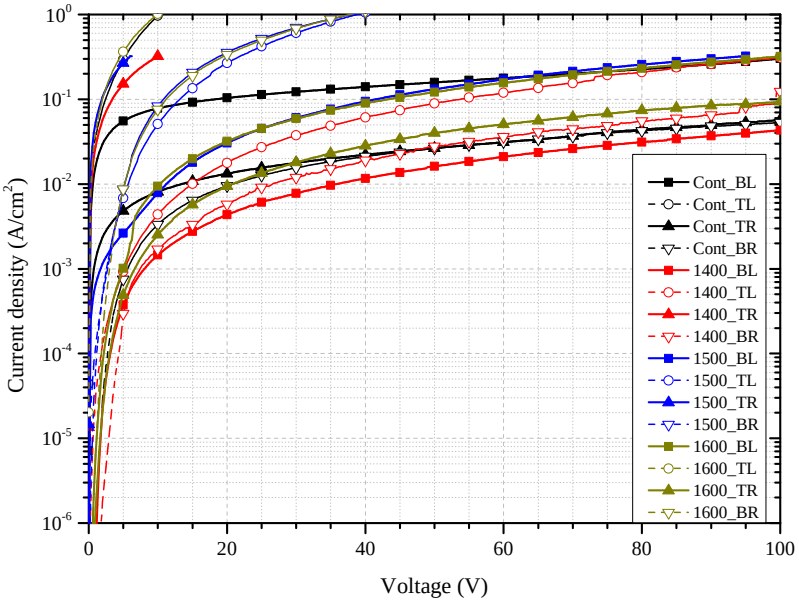


Figure 8.9: Reverse log(J)-V characteristics of first generation 10 kV PiN diodes at 25°C. The control sample, and the 1400°C, 1500°C and 1600°C oxidised samples are represented by black, red, blue and dark yellow traces respectively. Large-area device characteristics have solid markers and lines, whilst small-area device characteristics have open markers and dashed lines.

process has been experimentally incorporated into the second generation of 10 kV devices, presented in this Section. For this investigation, four 4H-SiC dies were used; two underwent the thermal oxidation and annealing process, and the remaining two were control samples. In order to obtain PiN diodes with four different active areas for both the oxidised and control samples, photolithography was performed using the DIE3 and DIE7 regions of the mask plates. With reference to Figure 8.2, the dies used were numbers 9 (control sample, DIE3), 13 (control sample, DIE7), 11 (oxidised sample, DIE3) and 31 (oxidised sample, DIE7). The dimensions of the PiN diodes fabricated in this Section are outlined in Table 8.3.

Table 8.3: Dimensions of second generation 10 kV PiN diodes.

Device size	Active area (cm^2)	Anode perimeter (cm)	P/A ratio
DIE3 (large)	0.0177	0.471	26.6
DIE3 (small)	0.0011	0.118	107.3
DIE7 (large)	0.0314	0.628	20
DIE7 (small)	0.0060	0.275	45.8

8.3.1 Novel Combined Thermal Oxidation and Annealing Process

The electrical characterisation results for the first generation of 10 kV 4H-SiC PiN diodes summarised in Table 8.1 and Table 8.2 indicated that, for a given oxidation time, performing the thermal oxidation at 1500°C yielded the most significant improvement in the on-state I(J)-V characteristics of the PiN diodes when compared against the control sample and measured at room temperature. However, these results also showed that the devices oxidised at 1600°C exhibited a greater improvement in their on-state characteristics when operated at 300°C. As such, it is difficult to conclude which temperature is optimum for the thermal oxidation process just from evaluating these results. However, it is expected that, for a given duration, performing the thermal oxidation at 1600°C should yield the greatest improvement in the on-state J-V characteristics of the fabricated PiN diodes. The reasoning for this is twofold. First, because the oxidation rate has been shown to increase with increasing temperature [57], the rate at which carbon interstitials diffuse into the semiconductor bulk is expected to correspondingly increase, thus more effectively repairing any carbon vacancy defects in the material. Secondly, as shown in [84], subjecting the 4H-SiC material to processing at 1600°C does not lead to any increased defect formation and subsequent carrier lifetime degradetion compared to processing at 1500°C. As such, the combined oxidation and annealing process that has been applied on

the second generation of 10 kV PiN diodes used an oxidation temperature of 1600°C.

As reported in [96], the thermal oxidation process results in an increase of the HK0 defect centre, which restricts the extent to which the carrier lifetime is increased. However, the HK0 defect was found to be eliminated after annealing in Ar at 1550°C for 30 minutes. This reduction of the HK0 defect centre was attributed to in-diffusion and/or out-diffusion of the carbon interstitials during the Ar anneal process. However, the Ar annealing was performed in a separate process to the thermal oxidation, thus adding considerable additional processing time and cost if it was to be implemented in a device fabrication process. As such, the Ar anneal process has been integrated with the high temperature thermal oxidation process using the Hitech dual-purpose furnace.

In the combined thermal oxidation and annealing process, cleaned dies were ramped up to the oxidation temperature of 1600°C at a rate of 8°C/min in an Ar atmosphere (5 l/min) where they were held for 15 minutes. The dies were then oxidised in dry pure oxygen (O_2) for 15 minutes at 1600°C, under an O_2 flow rate of 0.5 l/min. After the oxidation, the Ar flow was reinstated at 5 l/min, and the dies were ramped down to 1550°C and held there for an additional 30 minutes. After the Ar anneal hold, the dies were ramped down in temperature, again at 8°C/min, to 600°C, still in an Ar atmosphere. On removal from the furnace, the thermally-grown SiO_2 was then removed in dilute HF solution and the dies rinsed in DI water.

8.3.2 Fabrication Process

Samples first underwent the standard cleaning process outlined in Appendix B, then the combined thermal oxidation and annealing process described in Section 8.3.1 was applied to die numbers 11 and 31. Device mesas of ∼1.3 μm depth were defined using ICP etching,

using a TEOS SiO_2 and NiV mask. After the removal of the mesa mask, ~1.5 μm of TEOS SiO_2 was deposited for passivation; this was then patterned so that the ohmic contacts to the p-type anode could be formed. A Ti/Al metal scheme was used for the anode contact, and Ti/NiV was used for the cathode contact. The samples were then annealed using the RTA furnace at 1000°C for two minutes. Next, a 1 μm thick Al metal overlayer was deposited on the anode side and patterned using an Al wet etch solution. Finally, 10 nm of Ti and 500 nm layer of Ag was deposited onto the backside of the dies, to facilitate soldering to DCB substrates. After probe I-V measurements were completed, dies were soldered onto the DCB substrates using Ag solder heated to 230°C, and were ultrasonically wire bonded using 25 μm Al wire. In order to minimise the effect of bond wire resistance on the device characteristics, up to 10 parallel wires were bonded to each PiN diode, depending on the device contact pad area. A photograph of a DCB-mounted PiN diode die is shown in Figure 8.10.

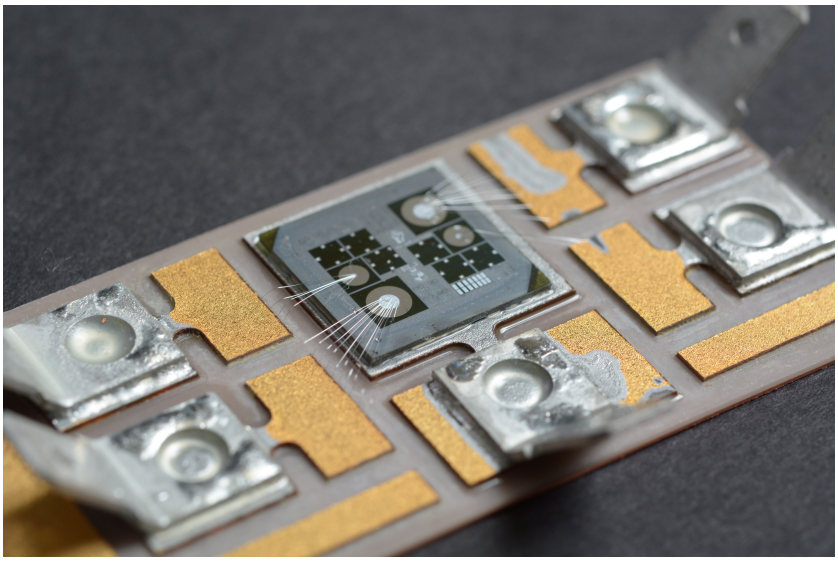


Figure 8.10: Photograph of DCB-mounted second-generation 10 kV PiN diode die.

8.3.3 Forward I-V Characterisation Results

As with the first generation of 10 kV PiN diodes, the forward I(J)-V characteristics of the second generation devices have been evaluated across the temperature range 25°C to 300°C, and up to 1 A current. For the DIE3 devices, this equates to a maximum current density of 909 A/cm^2 and 57 A/cm^2 for the small- and large-area devices respectively, and, for the DIE7 devices, 166 A/cm^2 and 32 A/cm^2 for the small- and large-area devices respectively. Pulsed-mode measurements were performed using four probes to minimise the effects of device self-heating and instrumentation resistance.

The forward J-V characteristics for the small-area devices from each of the four fabricated dies are shown in Figure 8.11. It can be seen that, as expected, the J-V characteristics generally improve with increasing temperature, although at current densities over 750 A/cm^2 (only measured on the DIE3 samples) the diode voltage drops at 300°C are only marginally lower than at 150°C. In addition, these results show that the combined thermal oxidation and annealing process has had a positive effect in reducing the voltage drop across the devices; for the DIE3 small-area diodes a reduction of 103 mV at 100 A/cm^2 and 25°C was observed, whilst for the DIE7 small-area diodes the voltage drop reduction was 240 mV.

A corresponding set of forward J-V characteristics for the large-area devices from each of the four fabricated dies is shown in Figure 8.12. Again, the samples that underwent the combined thermal oxidation and annealing process exhibit better forward characteristics than the control samples. However, from examining the results in Figures 8.11 and 8.12, it is evident that the larger the active area of the device, the higher the voltage drop is for a given current density. This is illustrated in Figure 8.13, which shows the mean forward voltage drop of the fabricated PiN diodes for each active area. It should be noted that

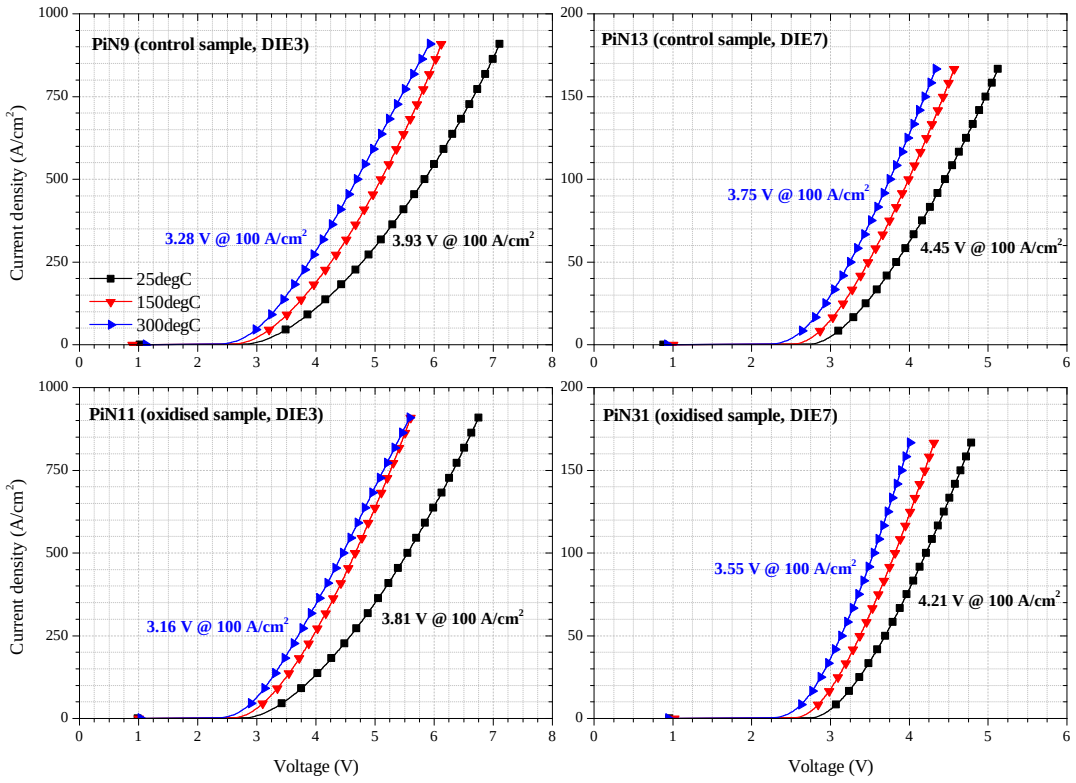


Figure 8.11: Forward J-V characteristics of small-area second generation 10 kV PiN diodes at 25°C, 150°C and 300°C.

the largest devices (0.0314 cm^2) have a wide error bar range due to two of the devices containing large triangular defects in their active areas (visible, and in correlation with Figure 8.2) and were therefore excluded from curve fitting; however, the remaining diode voltage drops were approximately in line with the linear fit. The fact that the larger devices have a higher forward voltage at a given current density contradicts the results presented in [143], who observed a higher forward voltage in devices with a small active area. This was attributed to enhanced recombination at the mesa perimeter, with the

small area devices with a high perimeter/area ratio having a higher forward voltage. From this, it can be deduced that recombination at the mesa perimeter has a negligible effect on the forward characteristics of the fabricated diodes; this in turn suggests that the mesa etch and passivation fabrication processes are effective in minimising the mesa surface recombination.

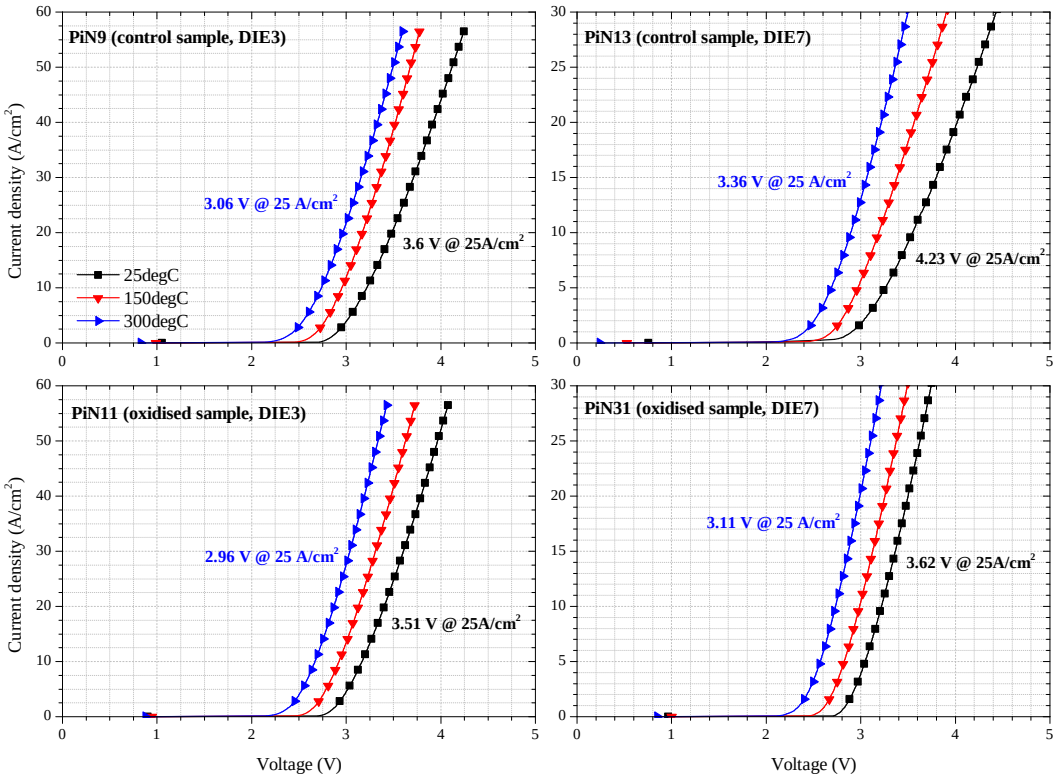


Figure 8.12: Forward J-V characteristics of large-area second generation 10 kV PiN diodes at 25°C, 150°C and 300°C.

Figure 8.14 shows the log(J)-V characteristics of selected small-area PiN diodes from both the control and oxidised DIE3 samples, at 25°C. It can be seen that the second

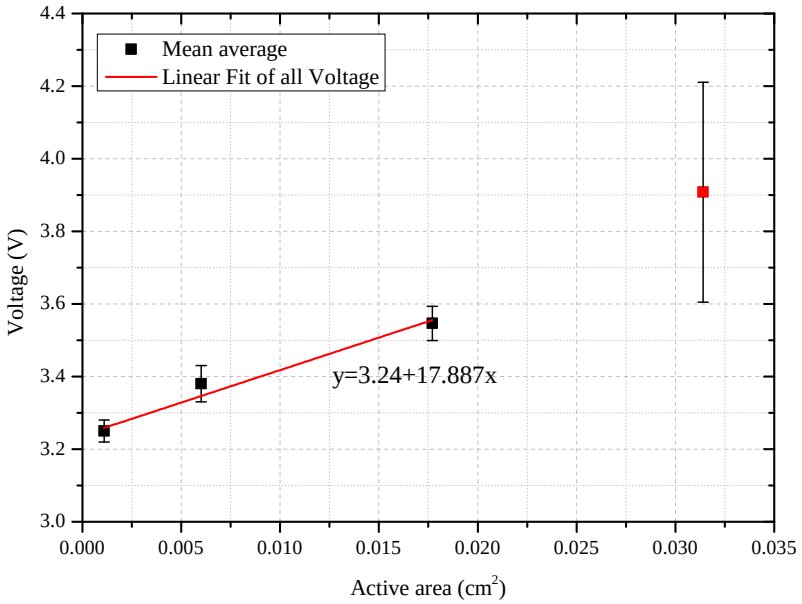


Figure 8.13: Forward voltage drop as a function of active area of second generation 10 kV PiN diodes. Data points used are from measurements taken at 25 A/cm^2 at 25°C.

generation of 10 kV PiN diodes have improved characteristics in the low-level injection region when compared with the first generation of 10 kV devices, which is beneficial for realising lower overall power losses. These improved characteristics are attributed to the use of a thicker TEOS SiO_2 passivation layer, preventing unintentional current conduction at the mesa sidewall. Shown inset in Figure 8.14 is the point of diode turn-on (around 2.6 V), where the ideality factor changes from 2 towards 1. The corresponding ideality factor against current density characteristic is shown in Figure 8.15. In contrast with the characteristics of the first generation 10 kV PiN diodes shown in Figure 8.7, the low-level injection regime has an ideality factor of approximately $\eta = 2$, indicating that recombination current dominates in these second generation devices. Beyond the onset of turn-on where diffusion current dominates, it can be seen that an ideality factor of

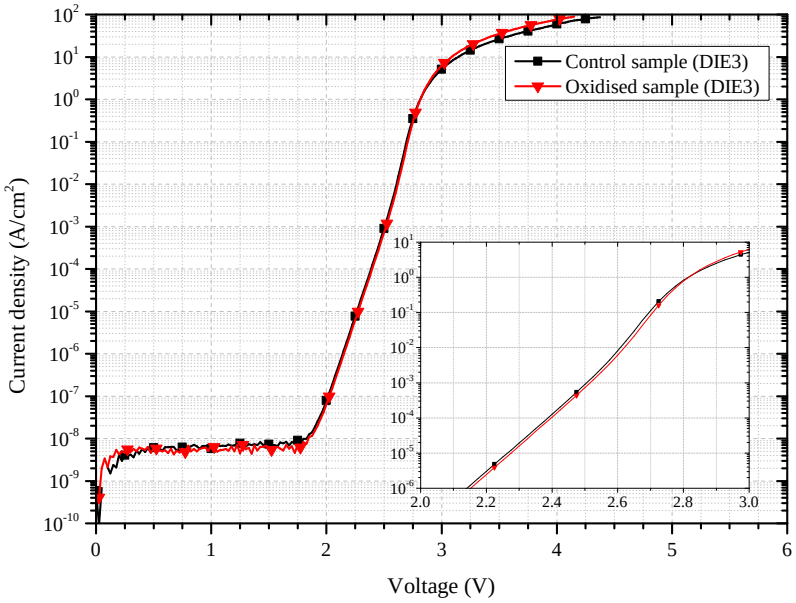


Figure 8.14: Log(J)-V characteristics of small-area second generation 10 kV PiN diodes at 25°C. The inset Figure shows the point of diode turn-on.

approximately $\eta = 1.5$ is attained, above the ideal value of $\eta = 1$.

Figures 8.16 and 8.17 show the differential on-state resistance as a function of current density for the small- and large-area PiN diodes respectively, at temperatures of 25°C, 150°C and 300°C. As expected, the resistance of the devices decreases dramatically with increasing forward bias due to the conductivity modulation effect, and, at high current densities, the resistance is generally lower at higher temperatures. However, unlike the first generation of 10 kV PiN diodes, the reduction in differential on-state resistance is generally negligible over 150°C. Furthermore, the characteristics of the small-area DIE3 devices show that at high current densities (approximately 450 A/cm^2 and 250 A/cm^2 for the control sample and oxidised sample respectively) the differential on-state resistance value becomes larger at 300°C than the corresponding value at 150°C.

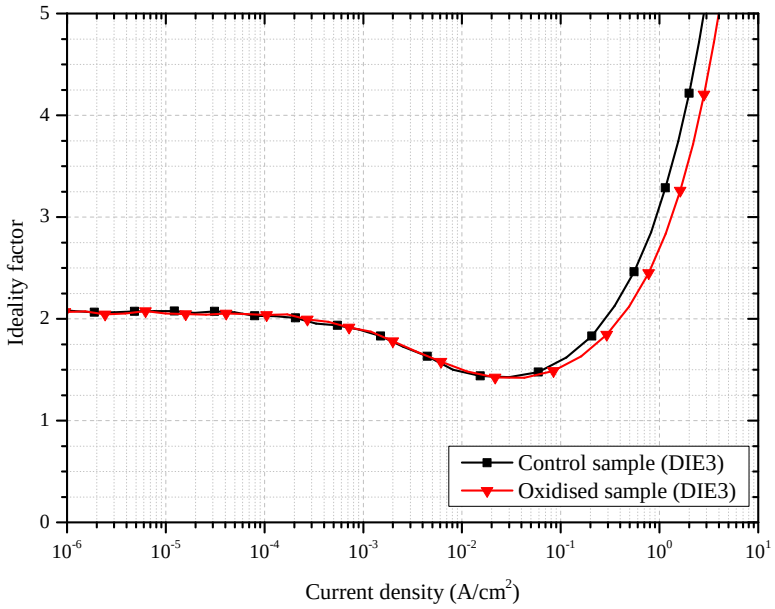


Figure 8.15: Ideality factor against current density of small-area second generation 10 kV PiN diodes at 25°C.

As was the case with the forward voltage drop of the fabricated PiN diodes, the results shown in Figures 8.16 and 8.17 illustrate that the differential on-state resistance of the devices increases with increasing active area. As these measurements were taken by probing direct to the die, prior to DCB mounting and wire bonding, it was suspected that this issue was due to insufficient current spreading at the anode contact. As such, this would be confirmed (or otherwise) by performing I-V measurements after mounting the PiN diode dies on the DCBs and wire bonding the anode contacts. In order to measure the forward I-V characteristics of the packaged PiN diodes, the Tektronix 371B high power curvetracer was used, in pulsed high-current mode. Sense terminals were used to minimise the effect of resistance of the measurement setup.

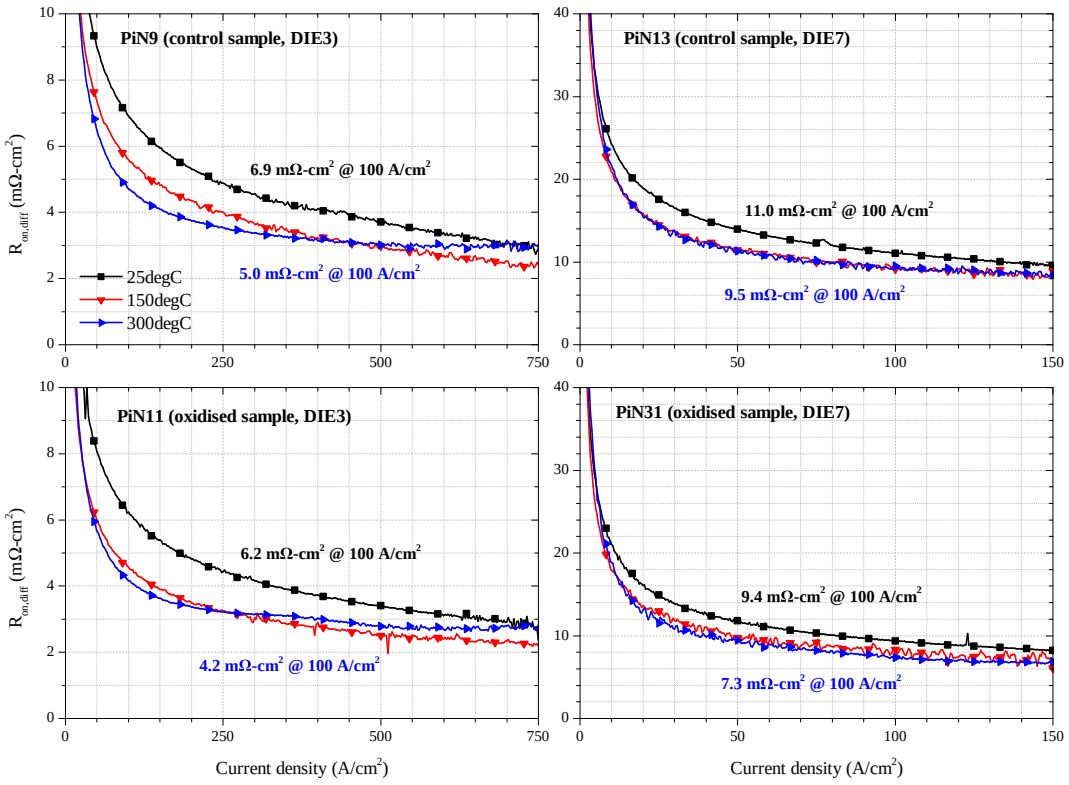


Figure 8.16: Differential on-resistance against current density of small-area second generation 10 kV PiN diodes at 25°C, 150°C and 300°C.

The collated statistical data for the extracted differential on-resistance of the DCB-mounted / wire bonded second generation 10 kV PiN diodes is illustrated in Figure 8.18. From this Figure it is evident that the values of differential on-resistance do not show the relationship with device active area as was observed with the probe measurements, which suggests that insufficient current spreading has been a problem with the previous generations of PiN diodes. Due to the large anode diameters, which in the fabricated large-area devices are up to 1.5 mm, the relatively small thickness of the Al metal overlayer

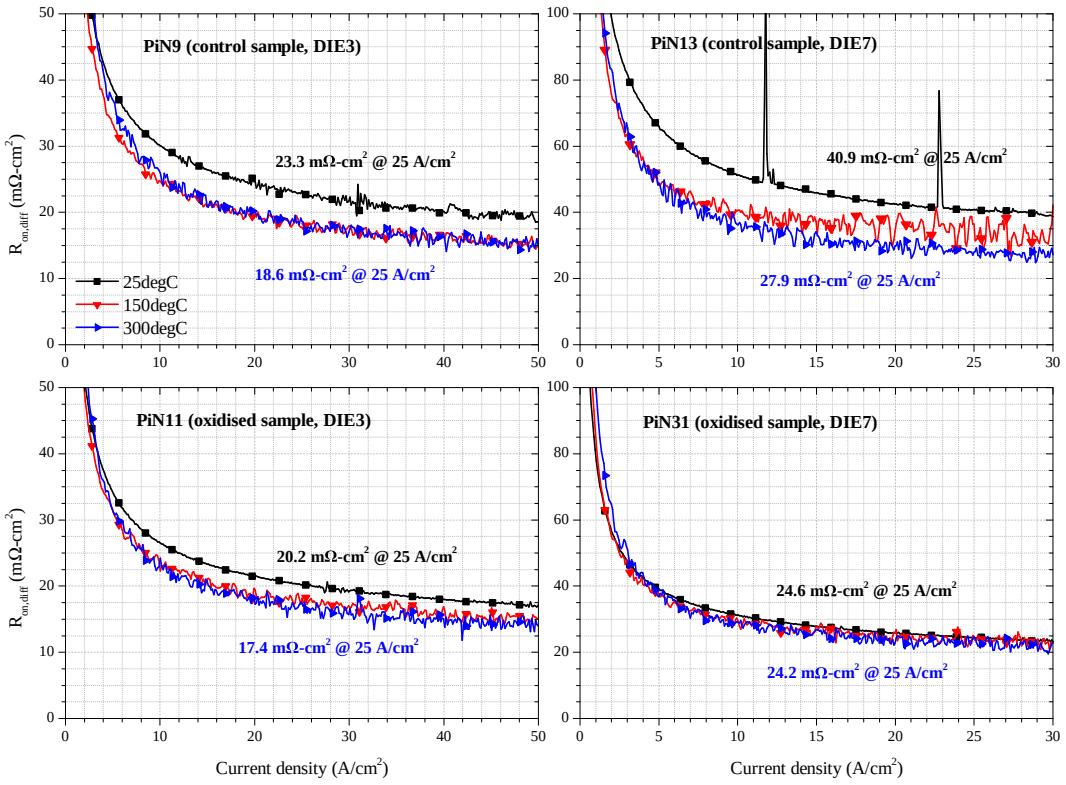


Figure 8.17: Differential on-resistance against current density of large-area second generation 10 kV PiN diodes at 25°C, 150°C and 300°C.

(1 μm) is the likely cause of this problem. In order to confirm this, numerical simulations of the PiN diode structure have been performed, using a anode contact of 50 μm to replicate the probe tip used in experimental measurements. Two different metal overlayer thickness have been simulated, the first was 1 μm thick and the second was 10 μm thick. The current density plots for these structures are shown in Figure 8.19. It is evident that the thickness of the metal overlay has a significant effect on the current spreading within the device structure, and the use of the 1 μm metal overlayer is shown to restrict the

majority of current flow to only underneath the anode contact, whilst the 10 μm metal overlayer clearly facilitates much greater lateral current flow. As such, thicker layers are clearly necessary if the performance of the devices are to be fully optimal, with the thickness of the layer being dependent on the lateral dimensions of the mesa anode.

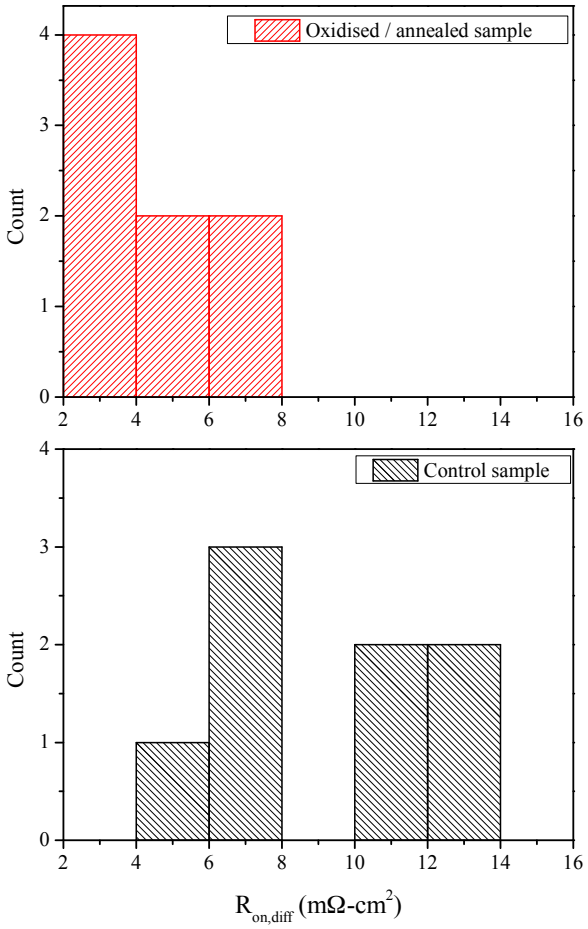
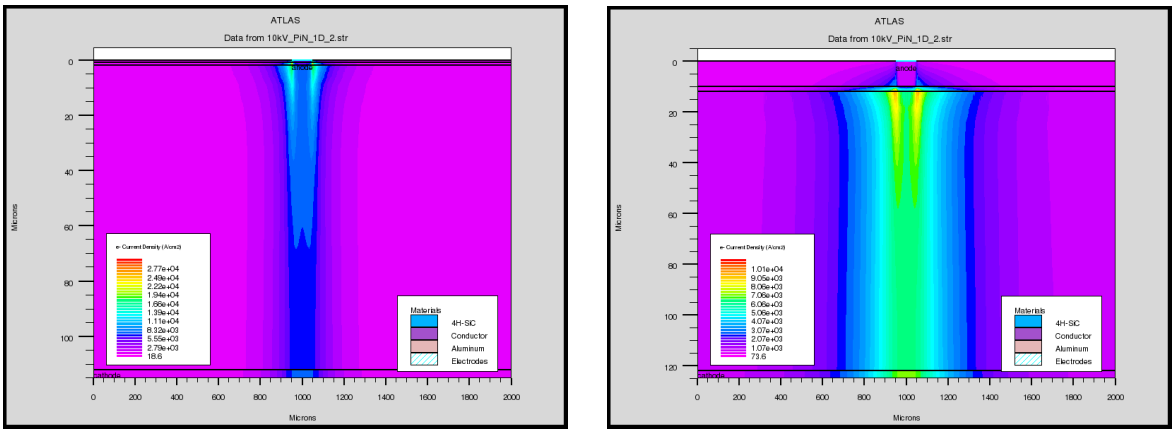


Figure 8.18: Statistical data for the differential on-resistance of DCB-mounted second generation 10 kV PiN diodes at 100 A/cm^2 and 25°C.

In addition to confirming the aforementioned issue with current spreading at the anode contact of the PiN diodes, Figure 8.18 also provides a clear comparison of the thermally oxidised / annealed sample PiN diodes and the control sample PiN diodes. It was found



(a) (b)

Figure 8.19: Numerical simulation of current density in PiN diode structures with (a) 1 μm and (b) 10 μm thick metal overlayers. The physical models and parameters described in Chapter 4 have been used for these simulations.

that the thermally oxidised / annealed sample PiN diodes had a mean differential on-resistance of 4.45 mΩ-cm^2, a standard deviation of 1.43 mΩ-cm^2, a minimum value of 3.0 mΩ-cm^2 and a maximum value of 7.1 mΩ-cm^2 at 100 A/cm^2. This compares to a mean differential on-resistance of 9.18 mΩ-cm^2, a standard deviation of 3.16 mΩ-cm^2, a minimum value of 5.3 mΩ-cm^2 and a maximum value of 13.9 mΩ-cm^2 for the control sample PiN diodes. This data clearly illustrates the on-state performance benefits that have been realised by incorporating the combined thermal oxidation / annealing process into the overall PiN diode fabrication process.

8.3.4 Clamped Inductive Switching Characterisation Results

Using the test equipment outlined in Section 5.1.3, the switching performance under inductive load conditions of the fabricated second generation 10 kV PiN diodes has been evaluated. For comparison, a 6.5 kV Si PiN diode die sourced from ABB [181] has been wire-bonded onto a DCB substrate and has undergone identical switching tests. The Si

IGBT (also a die wire-bonded to a DCB) used in the chopper cell circuit is rated for 6.5 kV and was also sourced from ABB. However, because the second generation of 10 kV PiN diodes have been fabricated without any edge termination, a relatively low DC bus voltage of 100 V has been used for these tests. Reverse breakdown measurements were performed on the fabricated PiN diodes using the Tektronix 371B curvetracer and devices were found to block in excess of 500 V (at 1 mA); however, it was also noted that the achieved blocking voltage was variable across different devices. As such, and due to the lack of second passivation layer over the metal overlay contacts on the dies, the relatively low voltage of 100 V was used.

In the chopper cell circuit used for these tests, shown in Figure 8.20, by using $\Delta T = 300\mu$s and $t_{on} = t_{off} = 20\mu$s, a peak inductor current of 400 mA was obtained. Data for V_{CE}, V_{GE}, V_{AK} and I_A was acquired using the digital oscilloscope at 250 Msamples/s, which equated to a sample resolution of 4.0 ns. The function generator used to provide the IGBT signal was operated in 1-cycle burst mode, and the oscilloscope was operated in single sequence capture mode triggering on the negative-edge of the V_{GE} signal at a level of 2.5 V.

Figures 8.21 and 8.22 shows the turn-on and turn-off characteristics of the Si PiN diode and Si IGBT under clamped inductive switching operation respectively. The IGBT turn-off is initiated by a decrease in V_{GE}; this initially falls exponentially as the gate-emitter capacitance C_{GE} and the gate-collector capacitance C_{GC} (collectively referred to as C_{iss}) are discharged. The V_{GE} then begins to plateau due to C_{GC} charging as the gate current I_G flows through it, thus allowing the collector-emitter voltage V_{CE} to increase. At this point, the diode turns on and the collector current I_C (the inverse of the diode current I_A) begins to fall; the IGBT can then sustain the required blocking voltage.

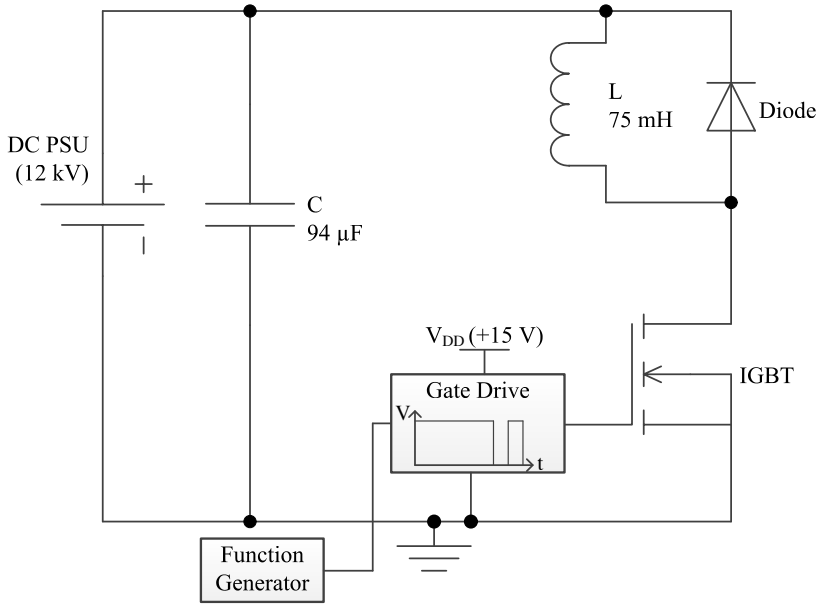


Figure 8.20: Schematic diagram of the chopper cell circuit used in for clamped inductive switching tests

Next addressing the IGBT turn-on / diode turn-off characteristics, V_{GE} first starts to increase and charge C_{iss}, though there is initially no other action since V_{GE} is less than the gate threshold voltage V_{TH}. Once V_{GE} exceeds the value of V_{TH}, the IGBT turns on and I_C starts to increase. However, before the PiN diode can support a reverse voltage, I_A reverses due to a negative applied voltage that appears across external stray inductance. After the reverse recovery current begins to flow, the diode voltage V_{AK} begins to increase until the diode can sustain the full reverse voltage. Figure 8.23 shows the power and energy dissipation of the Si PiN diode over the complete switching cycle, including turn-on, conduction and turn-off losses. It is clearly evident that the turn-off losses of the diode are the most significant, with the instantaneous power dissipation (P_{diode}) reaching around 220 W. For comparison, the steady state conduction P_{diode} is around 1.5 W and the turn-on P_{diode} reaches around 4 W. Over the complete switching

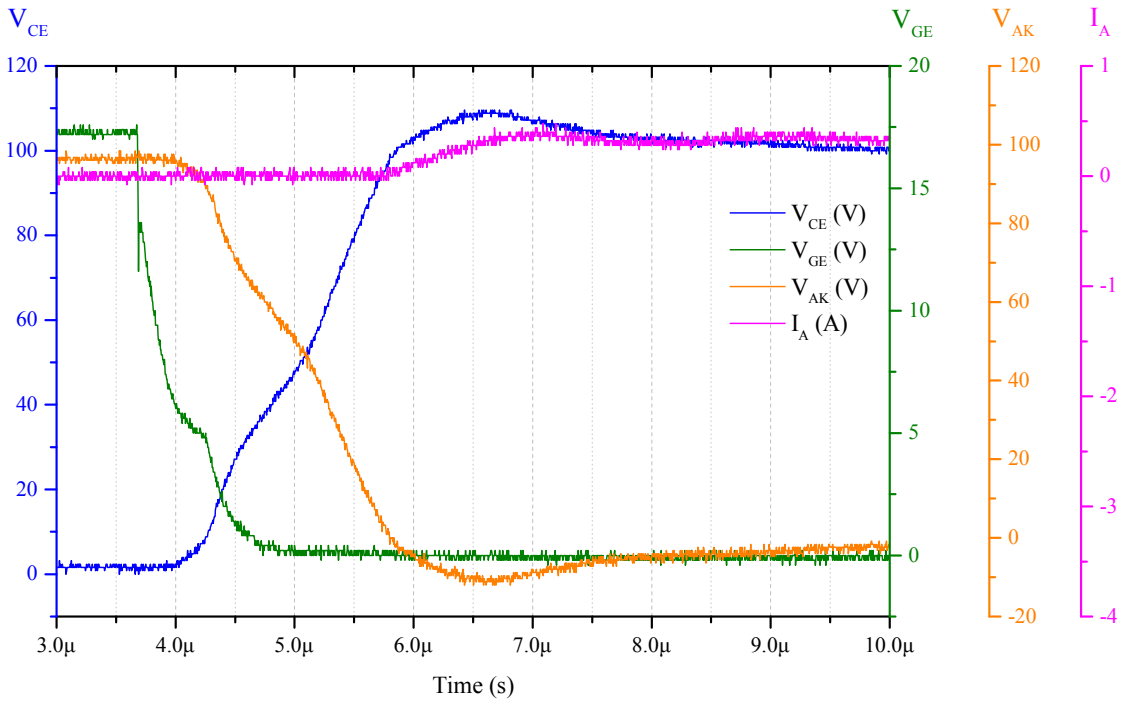


Figure 8.21: Inductive switching characteristics of Si diode and Si IGBT - IGBT turn-off, diode turn-on. Characteristics were measured at 25°C.

cycle this equates to an energy dissipation E_{diode} of around 60 μJ.

Figures 8.24 and 8.25 show the IGBT turn-off / diode turn-on and IGBT turn-on / diode turn-off for a fabricated 4H-SiC control sample PiN diode. First addressing the IGBT turn-off / diode turn-on characteristics, it can be seen that, when compared against the corresponding characteristics for the Si PiN diode, there is an increased overshoot of V_{CE} in the Si PiN diode circuit, peaking at 109.6 V. In contrast, there is a V_{CE} peak of 104 V in the 4H-SiC PiN diode circuit. This represents an overshoot of 9.6% and 4% for the Si PiN diode and the 4H-SiC PiN diode respectively. This overshoot in V_{CE} is attributed to additional parasitic inductance of the Si PiN diode (L_D), as all other circuit aspects remain the same. The implications of this increased overshoot in V_{CE} are twofold: first, the IGBT voltage gets closer to the breakdown voltage and thus needs to

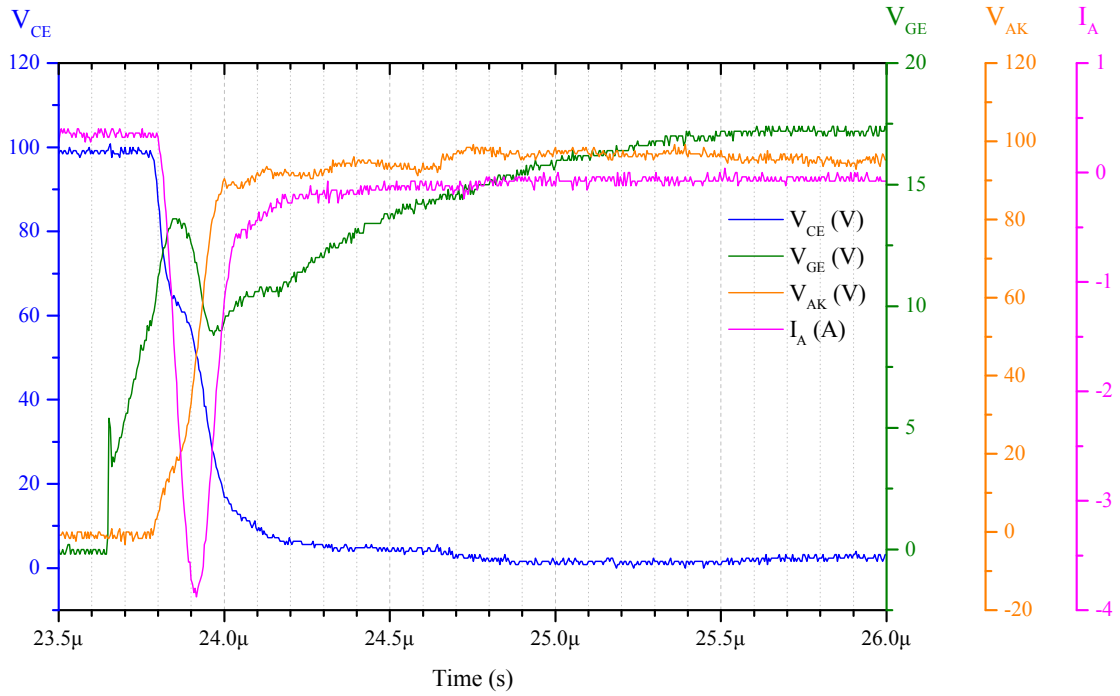


Figure 8.22: Inductive switching characteristics of Si diode and Si IGBT - IGBT turn-on, diode turn-off. Characteristics were measured at 25°C.

be operated at a lower DC bus voltage for a given device voltage rating, and second, the IGBT current falls slower, resulting in a larger turn-off energy loss.

Next comparing the IGBT turn-on / diode turn-off waveforms for the Si PiN diode and 4H-SiC PiN diode circuits, the increased L_D of the Si PiN diode results in a slower di/dt, more oscillations in V_{AK} and a reduced V_{CE} during the I_C rise (I_A fall). Moreover, it is clearly evident that the peak reverse current I_{RP} is much greater for the Si PiN diode, reaching around 3.9 A; this compares to around 1.2 A for the 4H-SiC PiN diode. The reverse recovery time t_{rr} is also longer for the Si PiN diode, being measured at 496 ns; this compares to 126 ns for the 4H-SiC PiN diode. The higher I_{RP} and the longer t_{rr} mean that the reverse recovery charge Q_{rr} is much greater for the Si PiN diode: a value of 575 nC was calculated from the experimental data for the Si PiN diode, whilst the

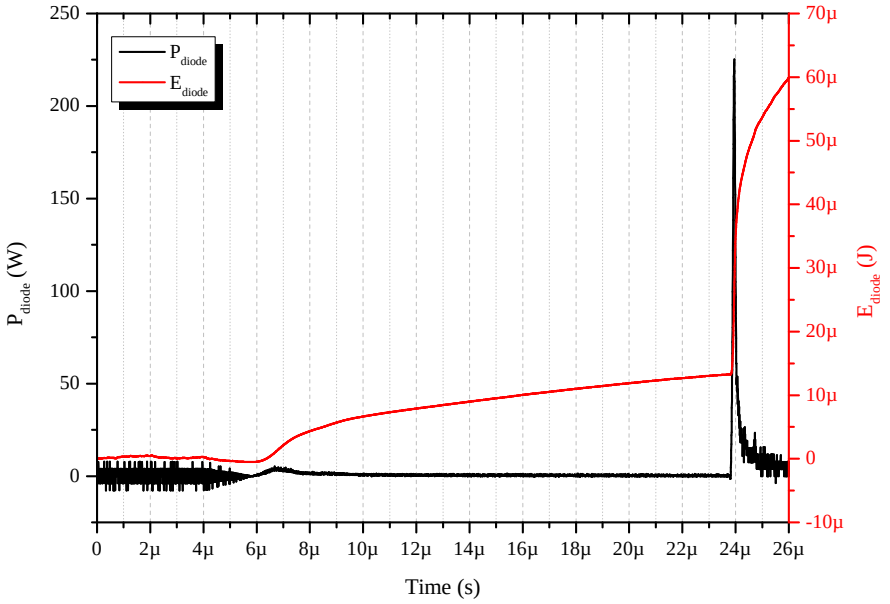


Figure 8.23: Power and energy dissipation of Si PiN diode over switching cycle at 25°C.

4H-SiC PiN diode was calculated to have a Q_{rr} of just 40 nC, a factor of more than 14 lower.

Figure 8.26 shows the power and energy dissipation of the 4H-SiC PiN diode over the complete switching cycle. As expected from the low Q_{rr} that was calculated, the turn-off energy is much lower than that for the Si PiN diode, being measured at around 6 μJ. It can be seen from this Figure that the dominant contributor to the overall PiN diode power losses are the conduction losses, which equate to an energy dissipation of around 20 μJ over the 20 μs on period. For comparison with the Si PiN diode, the instantaneous power dissipation of the 4H-SiC diode in the on-state is around 1 W, which is around 33% lower than that of the Si PiN diode. It is noted that some of this conduction loss is attributed to the wire bonding used for both PiN diodes; this could be improved by

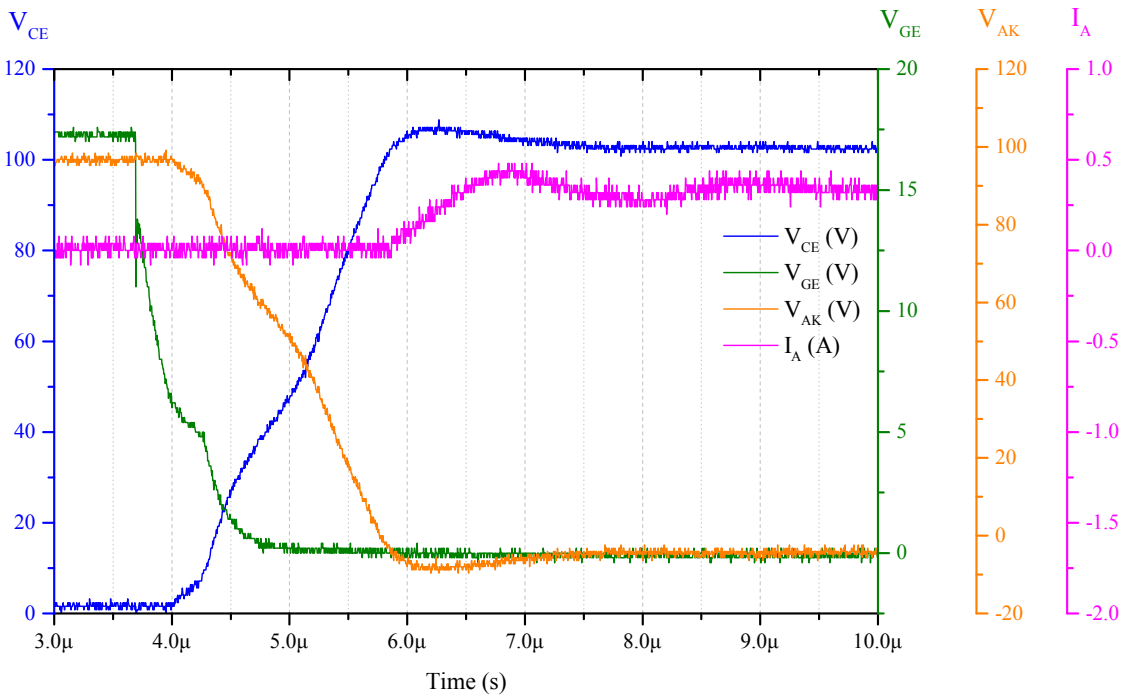


Figure 8.24: Inductive switching characteristics of SiC control sample PiN diode and Si IGBT - IGBT turn-off, diode turn-on. Characteristics were measured at 25°C.

the use of thicker bond wires and / or using more bond wires in parallel. The wiring to the PiN diode DCB also adds some series resistance to the diode (measured to be around 100 mΩ).

In addition to characterising the clamped inductive switching performance of the fabricated 4H-SiC PiN diodes and comparing them to commercial high voltage Si devices, the reverse recovery characteristics have also been used to estimate the carrier lifetime of the 4H-SiC devices using the Equation presented in Chapter 5, repeated here for ease [143]

$$\tau_{HL} = 2 \cdot t_{rr} \frac{I_{RP}}{I_F} \tag{8.2}$$

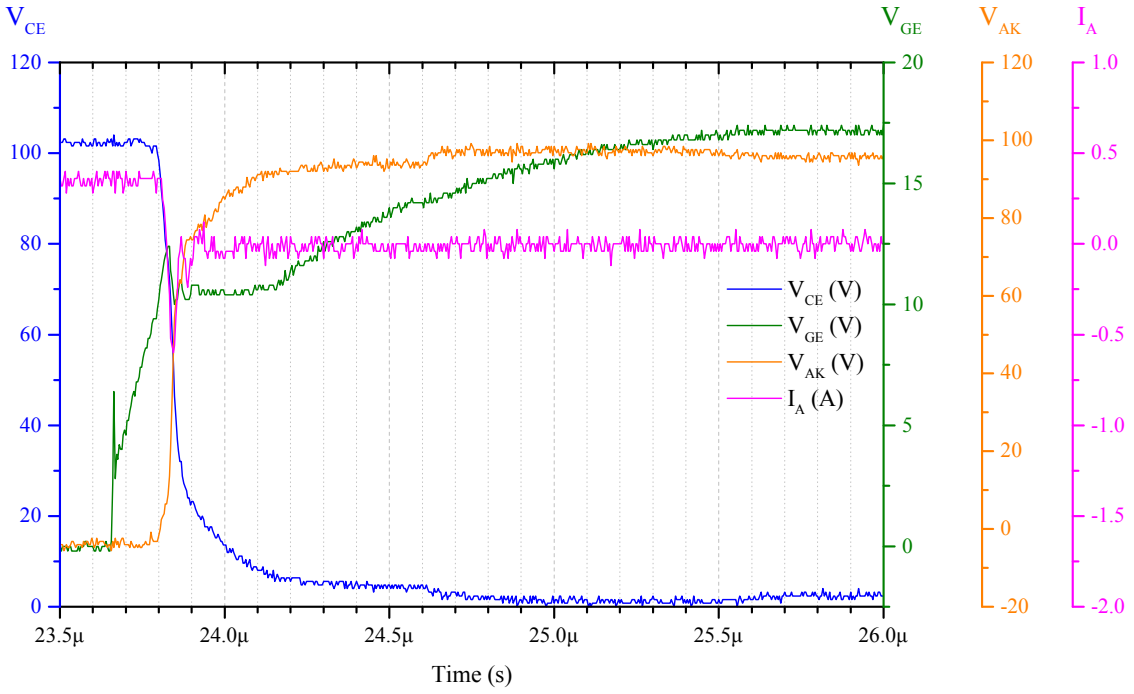


Figure 8.25: Inductive switching characteristics of SiC control sample PiN diode and Si IGBT - IGBT turn-on, diode turn-off. Characteristics were measured at 25°C.

Figure 8.27 shows the reverse recovery characteristics of selected control sample and thermally oxidised / annealed large-area PiN diodes. It can be seen that the thermally oxidised / annealed PiN diode has a slightly higher I_{RP} (1.5 A compared to 1.2 A) and longer t_{rr} (164 ns compared to 126 ns) than the control sample PiN diode. These reverse recovery characteristics equate to a Q_{rr} of 57 nC for the thermally oxidised / annealed PiN diode. Based on Equation 8.2, a τ_{HL} of 1.21 μs has been calculated for the thermally oxidised / annealed sample PiN diode; this compares to a value of 781 ns for the control sample PiN diode. These measurements indicate a 65% increase in the carrier lifetime of the device, though it is noted that this value of carrier lifetime achieved after performing the thermal oxidation / annealing process is still short of the 5 μs required for optimum performance of the PiN diodes fabricated in this Chapter.

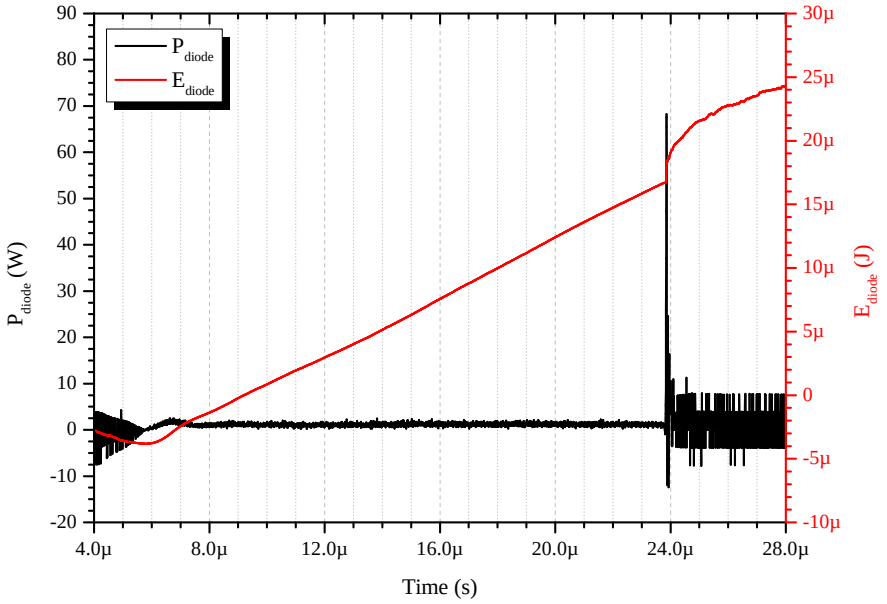


Figure 8.26: Power and energy dissipation of 4H-SiC PiN diode over switching cycle at 25°C.

8.4 Summary

In this Chapter, the fabrication and characterisation of PiN diodes designed for blocking 10 kV has been presented. After outlining the basic epitaxial structure of the devices and also the defect map for the 4H-SiC epitaxial wafer used for fabricating the devices in this Chapter, the first generation of PiN diodes were presented. In this generation of devices, high temperature thermal oxidation processes, at temperatures between 1400°C and 1600°C, were applied to PiN diodes with the aim of increasing the carrier lifetime and thus improving the forward characteristics of the devices. To the best of the author's knowledge, this is the first time such processes have been applied to 4H-SiC PiN diodes. Small-area control sample PiN diodes exhibited a forward voltage drop of 4.54 V at

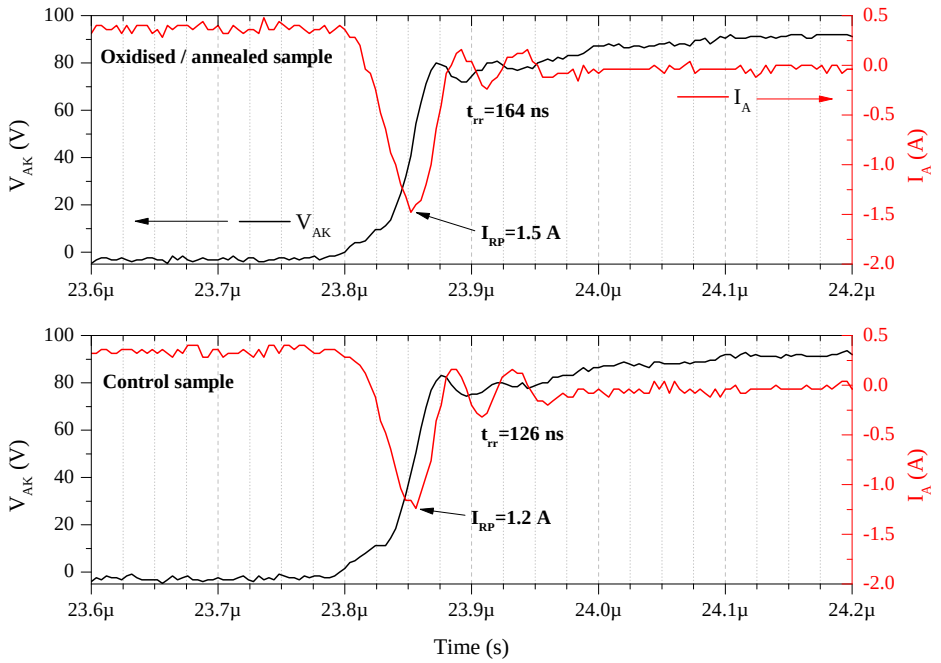


Figure 8.27: Reverse recovery characteristics of control sample (bottom) and oxidised / annealed sample (top) 4H-SiC large-area PiN diodes at 25°C.

100 A/cm^2 and 25°C, and a differential on-resistance of 11.6 mΩ-cm^2. However, in the low-level current regime the measured I-V characteristics were found to depart considerably from the ideal characteristics, which was attributed to a conduction path in parallel with the *pn* junction at the mesa sidewall. As a result of this, the measured reverse I-V characteristics were also rather poor, with the minimum reverse current density being measured at around 40 mA/cm^2.

In comparison with the first generation 10 kV control sample PiN diodes, the devices that underwent the high temperature thermal oxidation processes typically showed improved forward I-V characteristics, with the devices that were thermally oxidised at 1500°C yielding the best overall results. A differential on-resistance of 8.9 mΩ-cm^2 was measured for a typical small-area device, with a corresponding forward voltage drop of

4.15 V at 100 A/cm^2 and 25°C. However, it was observed from the complete set of results that the expected trend of decreasing differential on-resistance with increasing thermal oxidation wasn't definitive, suggesting that the variation in quality across the epitaxial material used for device fabrication considerably influences the performance of the devices. However, because the thermal oxidation times used for the fabrication of these devices were rather short (5 minutes), it is likely that device characteristics could be improved further by the use of a longer oxidation process time.

For the second generation 10 kV PiN diodes, a novel combined high temperature thermal oxidation / annealing process was developed and applied to 4H-SiC PiN diodes. Again, this is the first time such a process has been reported, to the best of the author's knowledge. Probe measurements on the dies showed that the PiN diodes that underwent the thermal oxidation / annealing process exhibited consistently better forward characteristics than the control sample PiN diodes, with a typical thermally oxidised / annealed small-area DIE3 device exhibiting a forward voltage drop of 3.81 V and a differential on-resistance of 6.2 mΩ-cm^2 (at 100 A/cm^2 and 25°C); both parameters were considerable improvements when compared to a corresponding control sample device. However, the problem of increasing differential on-resistance with increasing active area was observed; this was attributed to insufficient current spreading at the anode contact, and confirmed by means of numerical simulation and experimental measurements on DCB-mounted / wire bonded devices. The measurements that were performed after DCB mounting and wire bonding showed that across the complete set of devices, the thermally oxidised / annealed PiN diodes had a mean differential on-resistance of 4.45 mΩ-cm^2; this compared to 9.18 mΩ-cm^2 for the control sample PiN diodes. The forward characteristics of these thermally oxidised / annealed PiN diodes compare favourably to similar devices presented in the literature in recent years [127, 143].

By analysing the forward log(J)-V data for the second generation 10 kV PiN diodes, the devices were found to have ideal characteristics under low-level current injection ($\eta = 2$), illustrating that the previously-encountered problem where a conduction path in parallel with the *pn* junction was present had been resolved. However, in the diffusion current regime, where ideally $\eta = 1$, a slightly higher value of $\eta = 1.5$ was extracted, which was indicative of current transport being due to both diffusion and recombination mechanisms. It is likely that this is due to the quality of the epitaxial material used for device fabrication, though the possibility that these recombination centres were introduced during the overall device fabrication process cannot be ruled out.

Finally, clamped inductive switching tests were performed on the second generation 10 kV PiN diodes as well as on a commercial 6.5 kV Si PiN diode. As expected, the transient characteristics of the 4H-SiC devices were far superior, with a reverse recovery charge of just 40 nC (for a control sample 4H-SiC PiN diode) compared to 575 nC for the Si PiN diode. The thermally oxidised / annealed sample PiN diode had slightly worse transient characteristics than the control sample device, with a reverse recovery charge of 57 nC, though this was clearly much lower than the Si PiN diode. This slightly worse transient performance was due to the increase in carrier lifetime that was intended from carrying out the thermal oxidation / annealing process; a high-level lifetime of 1.21 μs was calculated from the reverse recovery characteristics. This compared to 781 ns for the control sample PiN diode, thus around a 65% increase.

Chapter

9 Conclusions and Future Work

In this final Chapter, the general conclusions of the research conducted in this thesis are presented. As a result of the conclusions that have been reached, several key areas that warrant further work have been outlined with the aim of further advancing the technological capability of high voltage 4H-SiC power electronics devices.

9.1 Conclusions

The overall aim of the research presented in this thesis was to advance the capability of 4H-SiC PiN diodes designed for high voltage applications, above 3.3 kV. Due to the nature of this research, the findings presented herein could similarly be applied to other 4H-SiC bipolar devices, such as IGBTS, BJTs and thyristors. Due to the clear advantages of using 4H-SiC rather than Si for power semiconductors, it is expected that this advancement of high voltage 4H-SiC bipolar devices will enable a transformation of not only the global power network, but also other applications, such as electric traction and industrial motor control.

From a power electronics application standpoint, the key parameter of a power semiconductor device is its efficiency, i.e. power losses need to be as small as possible. From the theoretical discussion presented in Chapter 3 it was illustrated that a sufficient carrier lifetime of the 4H-SiC material was crucial for realising low forward conduction losses of bipolar devices, with a lifetime of around 5 μs being required for devices designed for blocking 10 kV. As this value is typically much higher than as-grown 4H-SiC material, post-growth solutions for increasing the lifetime are necessary in order to achieve optimum forward conduction losses. However, the typically-low carrier lifetime of 4H-SiC is not the only reason for higher than expected forward conduction losses; the ohmic contacts, particularly to p-type material, can also add a considerable resistance to the overall series resistance of the device.

Because of the importance of forming a low resistance ohmic contact to p-type 4H-SiC, not to mention the considerable difficulty that was encountered in trying to achieve this task, a comprehensive investigation, which encapsulated both electrical and physical characterisation, was undertaken in order to try to understand the mechanisms behind the formation of reliable, low resistance ohmic contacts. This investigation was presented in Chapter 6, and the electrical characterisation of contact structures found that metal schemes employing Ti as the initial layer typically yielded the lowest specific contact resistance, with the Ti/Al scheme exhibiting the minimum specific contact resistance value achieved, which was around 2.2×10^{-6} Ω-cm^2. TEM analysis of the Ti/Al-based metal scheme prior to annealing showed that the Ti was epitaxially deposited on the 4H-SiC, whilst TEM analysis of the Ti/Al-based metal scheme after annealing showed the formation of what was suspected to be a Ti-based alloy. The TEM analysis of the annealed sample also illustrated the inhomogneous nature of the metal structure, a by-product of the anneal temperature being considerably higher than the Al melting point.

The XRD analysis that was performed on the range of p-type ohmic contact metal schemes showed that the Ti alloy Ti_3SiC_2 was a predominant feature of the XRD spectra of the annealed samples, though was found to be absent in the unannealed samples. The formation of this alloy, which is accepted for lowering the Schottky barrier at the metal-semiconductor interface, was found to be most prominent in the samples with Ti as the initial layer; this corresponded to the samples with the lowest values of specific contact resistance. Analysis of the current transport mechanisms in the contact structure using a model for TFE showed definite correlation between the values of specific contact resistance and the Schottky barrier height at the metal-semiconductor interface; in line with having the lowest measured specific contact resistance, the Ti/Al metal scheme exhibited the lowest Schottky barrier height, at 0.32 eV. Interestingly, ohmic contact structures that underwent a pre-anneal process at 600°C for 2 minutes showed improved electrical characteristics compared to samples that didn't have the pre-anneal; from the literature [160] it is suspected that this is due to enhanced silicide formation at the metal-semiconductor interface, though further investigation into this is warranted in order to confirm this.

After the development of the key fabrication processes discussed in Chapter 6 had reached a level deemed sufficient for device fabrication, the fabrication of PiN diodes designed for blocking 3.3 kV could commence. The first generation of 3.3 kV PiN diodes were fabricated without edge termination, as initially it was only the forward and (low-bias) reverse I-V characteristics that were of interest. Though the devices typically exhibited near-ideal characteristics, their forward voltage drop was fairly high, at around 4.8 V at 100 A/cm^2 and 25°C, as was $R_{on,diff}$, at around 17.0 mΩ-cm^2. An effective carrier lifetime of around 480 ns was calculated from the experimental measured data for the devices, which is typical of as-grown 4H-SiC material. Reverse I-V measurements showed that the

leakage current across the range of fabricated devices varied considerably, from 5 nA/cm^2 up to 200 μA/cm^2; because the fabricated devices underwent identical processing steps, this was attributed to the presence of defects in the 4H-SiC material.

During the fabrication of the first generation 3.3 kV PiN diodes, the use of a metal overlayer was investigated, as this would be needed for future device iterations that had to be wire bonded to DCB substrates. Upon characterising these devices with the metal overlayer it was evident that the device characteristics in the low-level injection regime had been adversely affected; this was attributed to the formation of a conduction path in parallel with the *pn* junction, which suggested that the oxide passivation layer had not fully coated the mesa sidewalls. This investigation also indicated that the use of the metal overlayer was beneficial for reducing the $R_{on,diff}$ of the PiN diodes, due to enhanced current spreading at the anode contact.

The second generation of 3.3 kV PiN diodes were fabricated with the SM-JTE structure numerically simulated in Chapter 4, with the aim of blocking 3.3 kV. Both the B implant profiles and the masking layer were designed using SRIM; three different implant doses were investigated (2.0×10^{13} cm^{-2} up to 8.0×10^{13} cm^{-2}), along with three different annealing temperatures (1500°C up to 1700°C). SIMS analysis showed that the as-implanted doping profile was in-line with the simulated profile, giving confidence in the SRIM simulation software used for implant designs. The doping profile of the sample annealed at 1500°C showed little difference from the as-implanted sample, illustrating that this annealing temperature was insufficient for activating the B atoms in the 4H-SiC. However, at 1600°C and 1700°C a considerable amount of B diffusion was observed. Also noteworthy is that, due to deficiencies in the equipment used for the activation annealing, the samples had unintentionally thermally oxidised during the process. Unexpectedly, the samples annealed with a TEOS SiO_2 capping layer were found to suffer more from

B out-diffusion. Both the TEOS-capped and the uncapped samples had oxidised during the anneal process, with the uncapped samples being found to have oxidised to a greater extent for a given annealing temperature. As such, it was concluded that this increased amount of oxidation resulted in an increased rate of carbon interstitials being generated at the oxidising surface of the 4H-SiC, which suppressed the B out-diffusion [141].

Further physical analysis of the B-implanted samples included DUV Raman spectroscopy, the aim of which was to analyse the effect of annealing temperature on the recovery of the 4H-SiC crystal after implantation. Unfortunately, due to the dopant out diffusion that had occurred during activation annealing, the Raman spectra for the annealed samples did not show the expected trend. The third and final physical characterisation technique employed to analyse the implanted samples was AFM, in order to determine the effect of the annealing processes on the surface morphology of the 4H-SiC samples. Across the range of annealing temperatures, the samples with the TEOS SiO_2 capping layer consistently showed worse surface roughness, possibly suggesting that the SiO_2 had converted to a crystalline phase and could not be removed in the HF etching process that was used after the anneal. The surface roughness of the uncapped samples annealed (thermally oxidised) at 1500°C and 1600°C showed similar characteristics, with an rms roughness of around 0.075 nm; the sample annealed at 1700°C was considerably worse than this, with a rms roughness of around 0.378 nm. From these results it was concluded that the use of thermal oxidation at 1700°C would result in a poor quality 4H-SiC/SiO_2 interface, which from a device performance perspective would be expected to yield poor electrical characteristics.

Electrical characterisation of the terminated PiN diodes illustrated that, in line with the results of the SIMS analysis, the 1500°C anneal process was insufficient for activating the B atoms, with consistently low breakdown voltages (less than 1000 V) being achieved.

As indicated by the numerical simulations performed in Chapter 4, the medium implant dose (4.0×10^{13} cm^{-2}) was the optimum of the three different doses experimented with for reverse breakdown performance, with a maximum blocking voltage of 2.8 kV being achieved. One final observation from these electrical characterisation results was that the samples annealed at 1700°C exhibited considerably worse reverse leakage current characteristics than the samples annealed at lower temperatures; it was concluded that this was due to the greater amount of B diffusion in the 4H-SiC bulk, resulting in a device structure that departed significantly from that which was intended.

The next Chapter focussed on the development of 4H-SiC PiN diodes with 110 μm drift regions, designed for blocking 10 kV. However, due to the ongoing problem of poor forward characteristics due to low carrier lifetimes in high voltage bipolar 4H-SiC devices, this Chapter focussed on the development of novel fabrication processes to improve the forward characteristics of PiN diodes. The first generation of 10 kV PiN diodes enabled a comparison of control sample devices against devices that had undergone thermal oxidation at temperatures ranging from 1400°C to 1600°C, for the relatively short process time of 5 minutes. Small-area control sample PiN diodes were found to have a typical forward voltage drop of 4.54 V and a $R_{on,diff}$ of 11.6 mΩ-cm^2 at 100 A/cm^2 and 25°C; the samples that had undergone the thermal oxidation process were found to improve on this, with a typical small-area PiN diode thermally oxidised at 1500°C having a forward voltage drop of 4.15 V and a $R_{on,diff}$ of 8.9 mΩ-cm^2 at 100 A/cm^2 and 25°C.

Though the results of the first generation 10 kV PiN diodes indicated that the thermal oxidation processes were effective in improving the forward characteristics of the devices, it was evident that, to some extent, the quality of the starting material was impacting the electrical performance that was observed. Moreover, deficiencies remained in the device fabrication process, resulting in poor characteristics under low-level injection conditions

and in reverse bias. It was concluded that this was due to same problem encountered in Chapter 7, in that the TEOS SiO_2 passivation was still not fully coating the mesa sidewalls. This problem was remedied in the second generation of 10 kV PiN diodes, by using a passivation layer considerably thicker than the mesa etch depth.

In attempting to further improve the forward characteristics of 10 kV PiN diodes, the second generation of devices underwent a novel combined high temperature thermal oxidation / annealing process. To the best of the author's knowledge, this was the first time such a process had been applied to any 4H-SiC device. As anticipated, the results of the thermally oxidised / annealed PiN diodes surpassed those of the second generation control sample devices as well as the thermally oxidised first generation 10 kV PiN diodes, with small-area devices exhibiting a forward voltage drop of 3.81 V and a $R_{on,diff}$ of 6.2 mΩ-cm^2 at 100 A/cm^2 and 25°C. In addition, the device characteristics at low-level injection were found to be near-ideal, as a result of the refined fabrication process. However, one problem was still prevalent in this generation of devices: the $R_{on,diff}$ increased with increasing device active area. Numerical simulation indicated that this was due to insufficient current spreading at the anode contact, in turn due to small metal overlayer thickness relative to the size of the anode contact. As such, it was concluded that to improve this aspect of device performance, a thicker metal overlayer, proportional in size to the anode contact diameter, is required.

Electrical measurements performed on DCB-mounted / wire-bonded PiN diodes yielded forward I-V results that were independent of the active area of the fabricated devices, the parallel wire bonds circumventing the problem of insufficient current spreading at the anode contact. These measurements showed that across the batch of thermally oxidised / annealed PiN diodes, a mean $R_{on,diff}$ value of 4.45 mΩ-cm^2 at 100 A/cm^2 and 25°C was achieved; this compared to 9.18 mΩ-cm^2 for the control sample PiN diodes. From

this significant improvement in the forward characteristics of the thermally oxidised / annealed devices, it can be concluded that the process is both an effective and efficient method of improving the performance of bipolar 4H-SiC devices; the results presented in this Chapter were found to compare favourably with recent results presented in the literature for similar devices [127, 143].

The final results Section of Chapter 8 presented the transient characteristics of the fabricated second generation 10 kV PiN diodes under clamped inductive switching conditions, and compared them against the transient characteristics of high voltage Si PiN diodes. As expected, the 4H-SiC PiN diodes performed significantly better under inductive switching conditions, with a reverse recovery charge around a factor of 14 lower than that of the Si device. A negligible difference in performance between the 4H-SiC control sample PiN diode and the thermally oxidised / annealed PiN diode was observed, though the thermally oxidised / annealed device exhibited slightly worse characteristics as a result of the increased carrier lifetime from the thermal oxidation / annealing process. From the device reverse recovery characteristics it was found that the carrier lifetime had increased from 781 ns in the control sample PiN diode, to 1.21 μs in the thermally oxidised / annealed device, an increase of around 65%. As such, it can be concluded that the novel combined high temperature thermal oxidation / annealing process is hugely beneficial for increasing the carrier lifetime in 4H-SiC.

9.2 Future Work

In this Section, areas for future research have been identified. There still remains huge scope for further improvements in high voltage 4H-SiC power semiconductor devices, these identified areas for future work aim to address this.

9.2.1 Device Modelling and Simulation

The numerical simulations of the devices in this thesis have been limited to 1- and 2-D analysis of forward I-V characteristics and reverse breakdown simulations of edge termination structures. Forward I-V simulations assumed ideal (zero resistance) ohmic contacts, and were all performed at 300 K. In future, for more comprehensive analysis of the behaviour of 4H-SiC device structures, it would be logical to incorporate the experimental findings in this thesis and use representative values for ohmic contacts, in particular those to p-type material. Furthermore, the carrier lifetime parameter, which strongly influences the characteristics of bipolar devices, should be also be set at to a value representative of that of typical 4H-SiC material.

Reverse breakdown simulations in this thesis solely focussed on 2-D structures, as, for most conventional semiconductor device structures, this can simultaneously yield accurate results whilst minimising computational time. However, for more elaborate JTE structures, which cannot be accurately modelled in 2-D, the use of 3-D simulations should be applied. One such example was presented towards the end of Chapter 4 (shown in Figure 4.24), where a graded JTE structure could be achieved by decreasing the mask spacings away from the *pn* junction; in order to accurately analyse the breakdown performance of this structure a 3-D simulation would be ideal.

It is apparent that in order to gain a complete picture of the device performance from the numerical simulations, the transient characteristics of the device also need to be simulated. This transient analysis was not undertaken in this thesis, due to issues with numerical convergence that were not resolved. As such, investigation into this is warranted in order to enable this analysis to take place. This will be beneficial for future 4H-SiC devices that are being designed, to demonstrate the on-state / switching performance

trade-off that results from varying the device parameters.

A final note to make regarding future work for 4H-SiC device modelling and simulation is the use of modelling for realisation of device structures, by simulating the fabrication processes using software such as Silvaco Athena. For the work presented in this thesis, it was considered that this was unnecessary, due to the relatively simple device structures that have been fabricated. In addition, due to the relative immaturity of 4H-SiC process modelling (compared to Si) and the resulting lack of comprehensive empirical data, the decision not to use process modelling was made. However, the amount of experimental data for 4H-SiC processing is continually accumulating, and process models for 4H-SiC are gradually becoming more robustly defined. As such, the use of these models could, in future, be used to obtain more accurate representations of device features, such as implanted edge termination regions. By using these process models, it would be expected that, in turn, more accurate electrical simulation results could be obtained.

9.2.2 Device Fabrication

Although significant progress was made in the device fabrication processes applied in this thesis, there still remains scope for further development to build on the experimental findings presented herein. Of huge importance to bipolar 4H-SiC devices is the formation of the ohmic contact to p-type material. In order to achieve more reproducible results in future, more accurate control of the RTA furnace used for the contact annealing is required, as the work presented in this thesis relied on manual control of the furnace. This resulted in variable ramp rates and temperature overshoot / undershoot, which no doubt had an impact on the electrical and physical characteristics of the fabricated contacts. A continued study into ohmic contacts is warranted, to further investigate the impact of

pre-annealing processes on the ohmic contact performance. Furthermore, the stability of these contacts should be investigated, if it is desired that the devices will operate at high temperature and under high current density. Further work should also address the issue of current spreading in the ohmic contacts; this will have a positive impact on the overall on-state power losses of 4H-SiC power devices.

A second aspect of device fabrication that still has vast scope for future development is the edge termination for high voltage 4H-SiC devices. One idea suggested in Chapter 4 but not yet applied in a fabricated device is that of the graded JTE structure, which could potentially be a simple yet high performance method for blocking high reverse voltages. Moreover, further experimentation with the implant dose could be worthwhile, to improve on the reverse blocking voltage capability that has already been achieved in this thesis. Finally, future work on implanted structures in 4H-SiC should ideally employ a RTA furnace; this should drastically reduce the problem of boron diffusion that was observed in Chapter 7.

Finally, it was clear from the results presented in Chapter 8 that the use of the novel combined high temperature thermal oxidation / annealing process was effective in enhancing the carrier lifetime in the 4H-SiC PiN diode and thus improving the forward characteristics of the fabricated devices. However, this process only applied a relatively short oxidation time of 15 minutes. Moreover, the oxidation rates at the high temperatures applied in this work are still little understood; as are the rates at which the 4H-SiC is consumed during the oxidation process. As such, further work in characterising these high temperature oxidation processes would be hugely beneficial, including performing the processes across a greater range of oxidation times.

9.2.3 Device Characterisation

Considering the characterisation of high voltage 4H-SiC power semiconductor devices, one particular area that still has considerable scope for future work is the clamped inductive switching characterisation of 4H-SiC devices at high voltage (∼10 kV) and at high temperatures (up to 300°C), in order to gain an understanding of how these devices will perform in the applications they are intended for. The test rig that was developed for this characterisation (discussed in Chapter 5) is capable of this, though due to only characterising the inductive switching performance of 4H-SiC devices without any edge termination, these capabilities were not utilised. This should be addressed in future generations of high voltage 4H-SiC devices, which have been fabricated with edge termination structures.

9.3 Final Words...

In the field of 4H-SiC power semiconductor devices, it is clear that, despite the excellent results published not only in this thesis but across the global research community, any 4H-SiC device is only ever as good as the starting material from which it is fabricated. Though great strides have been made in recent years in the field of material growth, huge variations in quality still exist, across vendors, and even across single substrates. As such, the material quality is undoubtedly key if 4H-SiC is ever going to fully reach its remarkable potential and penetrate the huge global power electronics markets as hoped. Encouragingly, an ever-growing number of vendors are now involved with the growth of 4H-SiC, this can only be a positive sign for the future of 4H-SiC in power electronics.

Appendix

A Fundamental Semiconductor Equations

The behaviour of semiconductor devices is governed by a number of fundamental variables and equations; these are outlined in this Appendix.

- Electric Field, $\mathscr{E}$ (V/cm):

$$E = -\nabla\psi \tag{A.1}$$

  where ψ is a scalar magnitude, known as the electrostatic potential (V).

- Poisson's Equation:

$$\nabla^2\psi = \nabla \cdot \mathscr{E} = \frac{q}{\varepsilon_S}(p - n + N_D - N_A) \tag{A.2}$$

  where ε_S is the static dielectric constant of the semiconductor, q is the electronic charge, N_D and N_A (cm^{-3}) are the doping concentrations of the n- and p-type semiconductor material respectively, and n and p (cm^{-3}) are the density of free electrons and holes respectively.

- Carrier Continuity Equations:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n - R + G \tag{A.3}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla \cdot J_p - R + G \tag{A.4}$$

where R and G are known as carrier recombination (where carriers annihilate each other) and generation (where carriers are generated as an electron-hole pair) respectively. Generation occurs in *impact ionisation* or *avalanche*. J_n and J_p are the electron and hole current densities ($\mathrm{A/cm^2}$) respectively.

- Carrier Transport Equations:

$$J_n = q\mu_n n\mathscr{E} + qD_n\nabla n \tag{A.5}$$

$$J_p = q\mu_p p\mathscr{E} + qD_p\nabla p \tag{A.6}$$

where the first terms on the right-hand side of the equations represent the drift currents and the second terms on the right-hand side represent the diffusion currents. μ_n and μ_p are the electron and hole mobilities, D_n and D_p are the electron and hole diffusion constants, which are related to their respective mobilities according to the Einstein relationship:

$$D_n = \frac{kT}{q}\mu_n \tag{A.7}$$

$$D_p = \frac{kT}{q}\mu_p \tag{A.8}$$

where k is Boltzmann's constant, T is temperature and q is the electronic charge. The electron and hole diffusion constants are in turn used to determine the ambipolar diffusion constant, given by

$$D_a = \frac{2D_nD_p}{(D_n + D_p)} \tag{A.9}$$

Appendix

B 4H-SiC Wafer Die Cleaning Process

B.1 Introduction

This Appendix details the 4H-SiC wafer die cleaning process that has been employed for all device fabrication work presented in the thesis.

B.2 Wafer Die Surface Cleaning Process

1. Place sample in acetone for 5 minutes in ultrasonic bath, rinse in deionised (DI) water and dry.

2. Place sample in isopropanol for 5 minutes in ultrasonic bath, rinse in DI water and dry.

3. Place sample in methanol for 5 minutes in ultrasonic bath, rinse in DI water and dry.

4. Place sample in 5% hydrofluoric (HF) acid solution for 1 minute, rinse in DI water.

5. Place sample in RCA Standard Clean (SC-1) solution (ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and DI water in the ratio 1:1:5) at a temperature in the range of 75 to 85°C for 10 minutes, rinse in DI water.

6. Place sample in 5% HF acid solution for 1 minute, rinse in DI water.

7. Place sample in RCA SC-2 solution (hydrochloric acid (HCl), H_2O_2 and DI water in the ratio 1:1:5) at a temperature in the range of 75 to 85°C for 10 minutes, rinse in DI water.

8. Place sample in 'Piranha' solution (sulphuric acid (H_2SO_4) and H_2O_2 in the ratio 3:1) for 10 minutes, rinse in DI water.

9. Place sample in 5% HF acid solution for 1 minute, rinse in DI water and dry.

Appendix

C Standard Photolithography Process

C.1 Introduction

This Appendix details the standard photolithography process that has been employed for all device fabrication work presented in the thesis.

C.2 Standard Photolithography Process

1. Using a pipette, deposit Primer onto the surface of the sample, leave for 1 minute, then blow dry with N_2 gun.

2. Place sample on spinner chuck, deposit S1818 photoresist using a pipette. Spin at 500 rpm for 1 second followed by 4000 rpm for 7 seconds.

3. Place sample on hot plate at 120°C for 3 minutes.

4. Expose sample on Karl Suss MJB3 mask aligner through edge bead removal photomask for 1.5 minutes.

5. Develop sample using MF319 solution for 50 seconds, rinse in DI water then dry.

6. Expose sample on Karl Suss MJB3 mask aligner through relevant layer photomask for 15 seconds.

7. Develop sample using MF319 solution for 30 seconds, rinse in DI water then dry.

8. Inspect sample using optical microscope for satisfactory feature definition.

Bibliography

[1] "http://www.eia.gov/forecasts/ieo/."

[2] M. R. Jennings, "Novel contact formation for 4H-SiC power devices," Ph.D. dissertation, University of Warwick, Coventry, UK, October 2007.

[3] M. R. Jennings, A. Pérez-Tomás, M. Davies, D. Walker, L. Zhu, P. Losee, W. Huang, S. Balachandran, O. J. Guy, J. A. Covington, T. P. Chow, and P. A. Mawby, "Analysis of Al/Ti, Al/Ni multiple and triple layer contacts to p-type 4H-SiC," *Solid-State Electronics*, vol. 51, pp. 797–801, 2007.

[4] T. Hiyoshi and T. Kimoto, "Reduction of deep levels and improvement of carrier lifetime in n-type 4H-SiC by thermal oxidation," *Applied Physics Express*, vol. 2, p. 041101, 2009.

[5] "http://unfccc.int/resource/docs/convkp/kpeng.pdf."

[6] "http://www.un.org/esa/population/publications/longrange2/worldpop2300final.pdf."

[7] "http://www.idtechex.com/research/articles/new-2012-forecasts-for-electric-vehicles-00004115.asp."

[8] V. K. Sood, *Power Electronics Handbook*. Burlington, USA: Elsevier, 2007, ch. 30 - HVDC Transmission, pp. 769–795.

[9] "http://www.siemens.com/innovation/en/news/2012/e_inno_1224_1.htm."

[10] N. Hadjsaid and J.-C. Sabonnadiere, *SmartGrids*. Hoboken, New Jersey, USA: Wiley, 2012.

[11] A. T. Bryant, E. Santi, J. Hudgins, and P. Palmer, *Power Electronics Handbook*. Burlington, USA: Elsevier, 2007, ch. 6 - Thyristors.

[12] "www.dynexsemi.com," December 2012.

[13] B. J. Baliga, "Enhancement- and depletion mode vertical-channel M.O.S. gated thyristors," *Electronics Letters*, vol. 15, no. 20, pp. 645–647, September 1979.

[14] "http://www.nationalgrid.com/nr/rdonlyres/7d099982-c937-4257-aeeb-6a7cd0757b79/50189/20100621_hvdc_detailed_factsheet_final.pdf."

[15] D. A. Guzman and J. C. Balda, "The impact of high-voltage and fast-switching devices on modular multilevel converters," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, Long Beach, CA, USA, 17-21 march 2013, pp. 2171–2177.

[16] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J.-K. Lim, M. Bakowski, L. Ängquist, and H.-P. Nee, "High-power modular multilevel converters with SiC JFETs," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 28–36, January 2012.

[17] H. H. G. Dunwoody, "Wireless telegraph system (patent)," December 1906.

[18] H. Baumhauer, "Über die kristalle des carborundums," *Z Kristallogr*, vol. 50, pp. 33–39, 1912.

[19] H. Baumhauer, "Über die verschiedenen modifikationen des carborundums und die erscheinung der polytypie," *Z Kristallogr*, vol. 55, pp. 249–259, 1915.

[20] J. A. Lely, "Darstelling von einkristallen von silizum carbid und beherrschung von art und menge der eingebauten verunreinigungen," *Ber. Dt. Keram. Ges.*, vol. 32, p. 299, 1955.

[21] Y. M. Tairov and V. F. Tsvetkov, "Investigation of growth processes of ingots of silicon carbide single crystals," *Journal of Crystal Growth*, vol. 43, pp. 1235–1236, 1978.

[22] H. Matsunami, S. Nishino, and H. Ono, "IVA-8 heteroepitaxial growth of cubic silicon carbide on foreign substrates," *IEEE Transactions on Electron Devices*, vol. 28, pp. 1235–1236, 1981.

[23] "http://www.cree.com."

[24] M. Bhatnagar, P. K. McLarty, and B. J. Baliga, "Silicon-carbide high-voltage (400 V) Schottky barrier diodes," *IEEE Electron Device Letters*, vol. 13, pp. 501–503, 1992.

[25] P. G. Neudeck, D. J. Larkin, J. A. Powell, L. G. Matus, and C. S. Salupo, "2000 V 6HSiC pn junction diodes grown by chemical vapor deposition," *Applied Physics Letters*, vol. 64, pp. 1386–1388, March 1994.

[26] O. Kordina, J. P. Bergman, A. Henry, E. Janzén, S. Savage, J. André, L. P. Ramberg, U. Lindefelt, W. Hermansson, and K. Bergman, "A 4.5 kV 6H silicon carbide rectifier," *Applied Physics Letters*, vol. 67, pp. 1561–1563, 1995.

[27] A. Itoh, T. Kimoto, and H. Matsunami, "High performance of high-voltage 4H-SiC Schottky barrier diodes," *IEEE Electron Device Letters*, vol. 16, no. 6, pp. 280–282, 1995.

[28] "http://www.infineon.com/cms/en/product/index.html."

[29] "http://www.microsemi.com."

[30] "http://www.ixys.com."

[31] D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, and K. Takatori, "Ultrahigh-quality silicon carbide single crystals," *Nature*, vol. 430, pp. 1009–1012, August 2004.

[32] "http://www.norstel.com/index.asp?p=home."

[33] "http://www.iiviwbg.com."

[34] "http://www.dowcorning.com/content/compsemi/."

[35] "http://www.tankeblue.com/index_en.html."

[36] "http://www.eetimes.com/electronics-news/4079657/industry-agrees-on-first-450-mm-wafer-standard."

[37] "http://www.cree.com/power/landing-pages/mosfet."

[38] "http://www.fairchildsemi.com."

[39] "http://www.rohm.com/web/global/."

[40] F. Bechstedt, P. Käckell, A. Zywietz, K. Karch, B. Adolph, K. Tenelsen, and J. Furthmüller, "Polytypism and properties of silicon carbide," *Physica Status Solidi (B)*, vol. 202, no. 35, pp. 35–62, 1997.

[41] R. Cheung, *Silicon carbide micro electromechanical systems for harsh environments*. Imperial College Press, 2006.

[42] S. M. Sze, *Physics of Semiconductor Devices*. Hoboken, New Jersey, USA: John Wiley and Sons, 1981.

[43] T. P. Chow, "Progress in high voltage SiC and GaN power switching devices," in *International Conference on Silicon Carbide and Related Materials (ICSCRM)*, Miyazaki, Japan, September 2013, pp. Mo–PL–2.

[44] F. Bauer, I. Nistor, A. Mihaila, M. Antoniou, and F. Udrea, "Superjunction IGBTs: An evolutionary step of silicon power devices with high impact potential," in *International Semiconductor Conference (CAS)*, vol. 1, Sinaia, Romania, 15-17 October 2012, pp. 27–36.

[45] C. Strenger, V. Häublein, T. Erlbacher, A. J. Bauer, H. Ryssel, A. M. Beltran, S. Schamm-Chardon, V. Mortet, E. Bedel-Pereira, M. Lefebvre, and F. Cristiano, "Comparative study of electrical and microstructural properties of 4H-SiC MOSFETs," *Materials Science Forum*, vol. 717-720, pp. 437–440, 2012.

[46] A. Powell, J. Jenny, S. Muller, H. M. Hobgood, V. Tsvetkov, R. Lenoard, and J. C. Carter, *SiC Materials and Devices: Growth of SiC Substrates*, M. Shur, S. Rumyantsev, and M. Levinshtein, Eds. Singapore: World Scientific, 2007, vol. 2.

[47] O. Kordina, C. Hallin, A. Ellison, A. S. Bakin, I. G. Ivanov, A. Henry, R. Yakimova, M. Touminen, A. Vehanen, and E. Janzén, "High temperature chemical vapor deposition of SiC," *Applied Physics Letters*, vol. 69, pp. 1456–1458, 1996.

[48] R. Yakimova, M. Syväjärvi, T. Iakimov, H. Jacobsson, R. Råback, A. Vehanen, and E. Janzén, "Polytype stability in seeded sublimination growth of 4H-SiC boules," *Journal of Crystal Growth*, vol. 217, no. 3, pp. 255–262, 2000.

[49] M. Syväjärvi, R. Yakimova, P. A. Glans, A. Henry, M. F. MacMillan, L. I. Johansson, and E. Janzén, "Morphology and polytype disturbances in sublimation growth of SiC epitaxial layers," *Journal of Crystal Growth*, vol. 198/199, no. 2, pp. 1019–1023, 1999.

[50] M. B. J. Wijesundara and R. Azevedo, *Silicon Carbide Microsystems for Harsh Environments*. Springer, 2011.

[51] H. Shiomi, H. Kinoshita, T. Furusho, T. Hayashi, M. Tajima, and E. Higashi, "Crystal growth of micropipe free 4H-SiC on 4H-SiC{0 3 $\overline{3}$ 8} seed and high-purity semi-insulating 6H-SiC," *Journal of Crystal Growth*, vol. 292, pp. 188–191, 2006.

[52] S. I. Maximenko, J. A. Freitas, Jr., R. L. Myers-Ward, K.-K. Lew, B. L. VanMil, C. R. Eddy, Jr., D. K. Gaskill, P. G. Muzykov, and T. S. Sudarshan, "Effect of threading screw and edge dislocations on transport properties of 4H-SiC homoepitaxial layers," *Journal of Applied Physics*, vol. 108, p. 013708, 2010.

[53] P. G. Neudeck, W. Huang, and M. Dudley, "Study of bulk and elementary screw dislocation assisted reverse breakdown in low-voltage (<250 V) 4H-SiC p^+n junction diodes - Part 1: DC properties," *IEEE Transactions on Electron Devices*, vol. 46, no. 3, pp. 478–484, March 1999.

[54] R. E. Stahlbush, M. Fatemi, J. B. Fedison, S. D. Arthur, L. B. Rowland, and S. Wang, "Stacking-fault formation and propagation in 4H-SiC PiN diodes," *Journal of Electronic Materials*, vol. 31, no. 5, pp. 370–375, 2002.

[55] R. E. Stahlbush, K. X. Liu, and M. E. Twigg, "Effects of dislocations and stacking faults on the reliability of 4H-SiC," in *IEEE 44th Annual International Reliability Physics Symposium*, San Jose, USA, 2006, pp. 90–94.

[56] "http://www.cree.com/news-and-events/cree-news/press-releases/2012/september/low-bpd-4hn-sic."

[57] S. M. Thomas, M. R. Jennings, Y. K. Sharma, C. A. Fisher, and P. A. Mawby, "Impact of oxidation temperature on the interface trap density in 4H-SiC MOS capacitors," in *International Conference on Silicon Carbide and Related Materials (ICSCRM)*, Miyazaki, Japan, October 2013.

[58] Y. K. Sharma, A. C. Ahyi, T. Isaacs-Smith, A. Modic, M. Park, Y. Xu, E. L. Garfunkel, S. Dhar, L. C. Feldman, and J. R. Williams, "High-mobility stable 4H-SiC MOSFETs using a thin PSG interfacial passivation layer," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 175–177, February 2013.

[59] H. Miyake, T. Kimoto, and J. Suda, "4H-SiC bipolar junction transistors with record current gains of 257 on (0001) and 335 on (000-1)," in *Proceedings of the 23rd International Symposium on Power Semiconductor Devices and IC's*, San Diego, CA, USA, May 2011, pp. 292–295.

[60] H. Miyake, T. Okuda, H. Niwa, T. Kimoto, and J. Suda, "21-kV SiC BJTs with space-modulated junction termination extension," *IEEE Electron Device Letters*, vol. 33, no. 11, pp. 1598–1600, November 2012.

[61] "http://www.genesicsemi.com."

[62] S. G. Sundaresan, A.-M. Soe, S. Jeliazkov, and R. Singh, "Characterization of the stability of current gain and avalanche-mode operation of 4H-SiC BJTs," *IEEE Transactions on Electron Devices*, vol. 59, no. 10, pp. 2795–2802, October 2012.

[63] "http://www.unitedsic.com."

[64] S. L. Rumyantsev, M. E. Levinshtein, M. S. Shur, L. Cheng, A. K. Agarwal, and J. W. Palmour, "High current (1300 A) optical triggering of a 12 kV 4H-SiC thyristor," *Semiconductor Science and Technology*, vol. 28, no. 045016, p. 3pp, 2013.

[65] L. Fursin, J. Hostetler, X. Li, A. Bhalla, F. Hoffmann, and M. Fox, "Breakthrough SiC GTOs enable efficient and compact next generation high voltage grid conversion," in *PCIM Europe*, Nuremberg, Germany, 14-16 May 2013, pp. 43–48.

[66] S.-H. Ryu, C. Capell, C. Jonas, L. Cheng, M. O'Loughin, A. Burk, A. Agarwal, A. Hefner, and J. Palmour, "Ultra high voltage(>12 kV), high performance 4H-SiC IGBTs," in *Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs*, Bruges, Belgium, 3-7 June 2012, pp. 257–260.

[67] H. Umezawa, M. Nagase, Y. Kato, and S.-I. Shikata, "High temperature application of diamond power device," *Diamond and Related Materials*, vol. 24, pp. 201–205, 2012.

[68] N. Kaminski and O. Hilt, "SiC and GaN devices - competition or coexistence?" in *International Conference on Integrated Power Electronics Systems (CIPS)*, Nuremberg, Germany, 6-8 March 2012, pp. 393–403.

[69] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York: Springer, 2008.

[70] W. Bartsch, R. Elpelt, R. Schoerner, K.-O. Dohnke, B. Bloecher, and K. Koerber, "Bipolar 6.5 kV-SiC-diodes: On the road to industrial application," in *European Conference on Power Electronics and Applications*, Dresden, Germany, 2005.

[71] T. Kimoto, K. Danno, and J. Suda, "Lifetime-killing defects in 4H-SiC epilayers and lifetime control by low-energy electron irradiation," *Physica Status Solidi (B)*, vol. 245, no. 7, pp. 1327–1336, 2008.

[72] K.-I. Matsushita, T. Shinohe, M. Tsukuda, Y. Minami, J.-I. Miwa, S. Yanagisawa, and H. Ohashi, "4.5 kV high-speed and rugged planar diode with novel carrier distribution control," in *Proceedings of the 1998 International Symposium on Power Semiconductor Devices and ICs*, Kyoto, Japan, 1998, pp. 191–194.

[73] P. Hazdra and V. Komarnitskyy, "Lifetime control in silicon power P-i-N diode by ion irradiation: Suppression of undesired leakage," *Microelectronics Journal*, vol. 37, pp. 197–203, 2006.

[74] P. A. Losee, C. Li, Y. Wang, S. K. Sharma, T. P. Chow, I. B. Bhat, R. E. Stahlbush, and R. J. Gutmann, "10kV 4H-SiC PiN diodes designed for improved switching performance using emitter injection control," in *Proceedings of the 19th International Symposium on Power Semiconductor Devices and ICs*, Cehju Isl, South Korea, May 2007, pp. 97–100.

[75] B. J. Baliga and S. K. Ghandhi, "Analytical solutions for the breakdown voltage of abrupt cylindrical and spherical junctions," *Solid-State Electronics*, vol. 19, pp. 739–744, 1976.

[76] P. Losee, "Design, fabrication and characterization of high voltage 4H-SiC junction rectifiers for power switching applications," Ph.D. dissertation, Rensselaer Polytechnic Institute, Troy, New York, USA, February 2007.

[77] D. C. Sheridan, G. Niu, J. N. Merrett, J. D. Cressler, C. Ellis, and C.-C. Tin, "Design and fabrication of planar guard ring termination for high-voltage SiC diodes," *Solid-State Electronics*, vol. 44, pp. 1367–1372, 2000.

[78] A. S. Kumta and X. Jinghua, "Field-plate-terminated 4H-SiC Schottky diodes using Al-based high-k dielectrics," *IEEE Transactions on Electron Devices*, vol. 56, no. 12, pp. 2925–2934, December 2009.

[79] M. Snook, T. McNutt, C. Kirby, H. Hearne, V. Veliadis, B. Nechay, S. Woodruff, R. S. Howell, J. White, and S. Davis, "Single photolithography/implantation 120-zone junction termination extension for high-voltage SiC devices," *Materials Science Forum*, vol. 717-720, pp. 977–980, 2012.

[80] T. Hiyoshi, T. Hori, J. Suda, and T. Kimoto, "Simulation and experimental study on the junction termination structure for high-voltage 4H-SiC PiN diodes," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1841–1846, August 2008.

[81] H. Niwa, G. Feng, J. Suda, and T. Kimoto, "Breakdown characteristics of 12-20 kV-class 4H-SiC PiN diodes with improved junction termination structures," in *Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs*, Bruges, Belgium, 3-7 June 2012.

[82] T. Seyller, "Passivation of hexagonal SiC surfaces by hydrogen termination," *Journal of Physics: Condensed Matter*, vol. 16, no. 17, pp. 1755–1782, 2004.

[83] I. D. Booker, J. Hassan, A. Hallén, E. Ö. Sveinbjörnsson, O. Kordina, and J. P. Bergman, "Comparison of post-growth carrier lifetime improvement methods for 4H-SiC epilayers," *Materials Science Forum*, vol. 717-720, pp. 285–288, 2012.

[84] B. Zippelius, J. Suda, and T. Kimoto, "On the formation of intrinsic defects in 4H-SiC by high temperature annealing steps," *Materials Science Forum*, vol. 717-720, pp. 247–250, 2012.

[85] A. Galeckas, J. Linnros, V. Grivickas, U. Lindefelt, and C. Hallin, "Auger recombination in 4H-SiC: Unusual temperature behaviour," *Applied Physics Letters*, vol. 71, no. 22, pp. 3269–3271, December 1997.

[86] R. J. Kumar, J. M. Borrego, R. J. Gutmann, J. R. Jenny, D. P. Malta, H. M. Hobgood, and C. H. Carter, Jr., "Microwave photoconductivity decay characterization of high-purity 4H-SiC substrates," *Journal of Applied Physics*, vol. 102, p. 013704, 2007.

[87] N. Achtziger and W. Witthuhn, "Band gap states of Ti, V, and Cr in 4H-silicon carbide," *Applied Physics Letters*, vol. 71, no. 1, pp. 110–112, 1997.

[88] L. Storasta, F. H. C. Carlsson, S. G. Sridhara, J. P. Bergman, A. Henry, T. Egilsson, A. Hallén, and E. Janzén, "Pseudodonor nature of the D_i defect in 4H-SiC," *Applied Physics Letters*, vol. 78, no. 1, pp. 46–48, 2001.

[89] J. Zhang, L. Storasta, J. P. Bergman, N. T. Son, and E. Janzén, "Electrically active defects in n-type 4H-silicon carbide grown in a vertical hot-wall reactor," *Journal of Applied Physics*, vol. 93, no. 8, pp. 4708–4714, 2003.

[90] J. Schneider, H. D. Müller, K. Maier, W. Wilkening, and F. Fuchs, "Infrared spectra and electron spin resonance of vanadium deep level impurities in silicon carbide," *Applied Physics Letters*, vol. 56, no. 12, pp. 1184–1186, 1990.

[91] B. Zippelius, A. Glas, H. B. Weber, G. Pensl, T. Kimoto, and M. Krieger, "$Z_{1/2}$- and EH_6 in 4H-SiC: Not identical defects?" *Materials Science Forum*, vol. 717-720, pp. 251–254, 2012.

[92] K. Danno and T. Kimoto, "Deep level transient spectroscopy on as-grown and electron-irradiated p-type 4H-SiC epilayers," *Journal of Applied Physics*, vol. 101, no. 10, pp. 3704–5, 2007.

[93] K. Danno, T. Kimoto, and H. Matsunami, "Midgap levels in both n- and p-type 4H-SiC epilayers investigated by deep level transient spectroscopy," *Applied Physics Letters*, vol. 86, p. 122104, 2005.

[94] L. Storasta and H. Tsuchida, "Reduction of traps and improvement of carrier lifetime in 4H-SiC epilayers by ion implantation," *Applied Physics Letters*, vol. 90, p. 062116, 2007.

[95] T. Miyazawa, M. Ito, and H. Tsuchida, "Evaluation of long carrier lifetimes in thick 4H silicon carbide epitaxial layers," *Applied Physics Letters*, vol. 97, no. 202106, 2010.

[96] T. Hiyoshi and T. Kimoto, "Elimination of the major deep levels in n- and p-type 4H-SiC by two-step thermal treatment," *Applied Physics Express*, vol. 2, p. 091101, 2009.

[97] J. W. Palmour, R. F. Davis, T. Wallett, and K. B. Bhasin, "Dry etching of βSiC in CF_4 and CF_4+O_2 mixtures," *J. Vac. Sci. Technol. A*, vol. 4, no. 3, pp. 590–593, 1986.

[98] P. H. Yih and A. J. Steckl, "Residue-free reactive ion etching of silicon carbide in fluorinated plasmas: II," *Journal of the Electrochemical Society*, vol. 142, no. 1, pp. 312–319, 1995.

[99] L. Cao, B. Li, and J. H. Zhao, "Etching of SiC using inductively coupled plasma," *Journal of the Electrochemical Society*, vol. 145, no. 10, pp. 3609–3612, 1998.

[100] J. H. Zhao, P. Alexandrov, and X. Li, "Demonstration of the first 10-kV 4H-SiC Schottky barrier diodes," *IEEE Electron Device Letters*, vol. 24, no. 6, pp. 402–404, June 2003.

[101] J. Wu, L. Fursin, Y. Li, P. Alexandrov, M. Weiner, and J. H. Zhao, "4.3 kV 4H-SiC merged PiN/Schottky diodes," *Semiconductor Science Technology*, vol. 21, pp. 987–991, June 2006.

[102] "http://www.srim.org," May 2013.

[103] T. Ayalew, "SiC semiconductor devices - technology, modeling, and simulation," Ph.D. dissertation, Technische Universität Wien Institute for Microelectronics, Austria, January 2004.

[104] G. Pensl, F. Ciobanu, T. Frank, M. Krieger, S. Reshanov, F. Schmid, and M. Weidner, "SiC material properties," *International Journal of High Speed Electronics and Systems*, vol. 15, no. 4, pp. 705–745, 2005.

[105] M. A. Capano, R. Santhakumar, R. Venugopal, M. R. Melloch, and J. A. Cooper, Jr., "Phosphorus implantation into 4H-silicon carbide," *Journal of Electronic Materials*, vol. 29, no. 2, pp. 210–214, 2000.

[106] A. Hallén, A. Henry, P. Pellegrino, B. G. Svensson, and D. Åberg, "Ion implantation induced defects in epitaxial 4H-SiC," *Materials Science and Engineering*, vol. B61-62, pp. 378–381, 1999.

[107] A. Schöner, *Process technology for silicon carbide devices*, C.-M. Zetterling, Ed. London, UK: IEE INSPEC, 2002.

[108] S. Seshadri, G. W. Eldridge, and A. K. Agarwal, "Comparison of the annealing behaviour of high-dose nitrogen-, aluminum-, and boron-implanted 4H-SiC," *Applied Physics Letters*, vol. 72, no. 16, pp. 2026–2028, 1998.

[109] E. M. Handy, M. V. Rao, K. A. Jones, M. A. Derenge, P. H. Chi, R. D. Vispute, T. Venkatesan, N. A. Papanicolaou, and J. Mittereder, "Effectiveness of AlN encapsulant in annealing ion-implanted SiC," *Journal of Applied Physics*, vol. 86, no. 2, pp. 746–751, 1999.

[110] K. V. Vassilevski, N. G. Wright, I. P. Nikitina, A. B. Horsfall, A. G. O'Neill, M. J. Uren, K. P. Hilton, A. G. Masterton, A. J. Hydes, and C. M. Johnson, "Protection of selectively implanted and patterned silicon carbide surfaces with graphite capping layer during post-implantation annealing," *Semiconductor Science Technology*, vol. 20, pp. 271–278, 2005.

[111] M. Rawski, J. Żuk, M. Kulik, A. Droździel, L. Lin, S. Prucnal, K. Pyszniak, and M. Turek, "Influence of hot implantation on residual radiation damage in silicon carbide," *Acta Physica Polonica A*, vol. 120, no. 1, pp. 192–195, 2011.

[112] C. Hallin, R. Yakimova, B. Pécz, A. Georgieva, T. S. Marinova, L. Kasamakova, R. Kakanakov, and E. Janzén, "Improved Ni ohmic contact on n-type 4H-SiC," *Journal of Electronic Materials*, vol. 26, no. 3, pp. 119–122, 1997.

[113] Y. Gao, Y. Tang, M. Hoshi, and T. P. Chow, "Improved ohmic contact on n-type 4H-SiC," *Solid-State Electronics*, vol. 44, pp. 1875–1878, 2000.

[114] S. Y. Han, K. H. Kim, J. K. Kim, H. W. Jang, K. H. Lee, N.-K. Kim, E. D. Kim, and J.-L. Lee, "Ohmic contact formation mechanism of Ni on *n*-type 4H-SiC," *Applied Physics Letters*, vol. 79, no. 12, pp. 1816–1818, 2001.

[115] L. M. Porter and R. F. Davis, "A critical review of ohmic and rectifying contacts for silicon carbide," *Materials Science and Engineering*, vol. B34, no. 2-3, pp. 83–105, 1995.

[116] F. Roccaforte, F. L. Via, and V. Raineri, "Ohmic contacts to SiC," *International Journal of High Speed Electronics and Systems*, vol. 15, no. 4, pp. 781–820, 2005.

[117] M. Siad, M. Abdesslam, and A. C. Chami, "Role of carbon in the formation of ohmic contact in Ni/4H-SiC and Ni/Ti/4H-SiC," *Applied Surface Science*, vol. 258, pp. 6819–6822, 2012.

[118] B. J. Johnson and M. A. Capano, "Mechanism of ohmic behavior of Al/Ti contacts to p-type 4H-SiC after annealing," *Journal of Applied Physics*, vol. 95, no. 10, pp. 5616–5620, 2004.

[119] A. Y. C. Yu, "Electron tunneling and contact resistance of metal-silicon contact barriers," *Solid-State Electronics*, vol. 13, pp. 239–247, 1970.

[120] Z. Wang, M. Saito, S. Tsukimoto, and Y. Ikuhara, "Terraces at ohmic contact in SiC electronics: Structure and electronic states," *Journal of Applied Physics*, vol. 111, p. 113717, 2012.

[121] F. Roccaforte, A. Frazzetto, G. Greco, F. Giannazzo, P. Fiorenza, R. L. Nigro, M. Saggio, M. Leszczyński, P. Pristawko, and V. Raineri, "Critical issues for interfaces to p-type SiC and GaN in power devices," *Applied Surface Science*, vol. 258, pp. 8324–8333, 2012.

[122] K. Nakayama, A. Tanaka, K. Asano, T. Miyazawa, and H. Tsuchida, "Influence of in-grown stacking faults on electrical characteristics of 4H-SiC PiN diode with long carrier lifetime," *Materials Science Forum*, vol. 740-742, pp. 903–906, 2013.

[123] D. Okamoto, Y. Tanaka, N. Matsumoto, M. Mizukami, C. Ota, K. Takao, K. Fukuda, and H. Okumura, "Development of high-voltage 4H-SiC PiN diodes on 4° and 8° off-axis substrates," *Materials Science Forum*, vol. 740-742, pp. 907–910, 2013.

[124] B. Kallinger, P. Berwian, J. Friedrich, C. Hecht, D. Peters, P. Friedrichs, and B. Thomas, "SXRT investigations on electrically stressed 4H-SiC PiN diodes for 6.5 kV," *Materials Science Forum*, vol. 740-742, pp. 899–902, 2013.

[125] G. Civrac, F. Laariedh, N. Theirry-jebali, M. Lazar, D. Planson, P. Brosselard, J. ul Hassan, A. Henry, E. Janzén, B. Vergne, and S. Scharnholz, "600 V PiN diodes fabricated using on-axis 4H silicon carbide," *Materials Science Forum*, vol. 717-720, pp. 969–972, 2012.

[126] J. Hassan, J. P. Bergman, A. Henry, and E. Janzén, "In-situ surface preparation of nominally on-axis 4H-SiC substrates," *Journal of Crystal Growth*, vol. 310, no. 20, pp. 4430–4437, 2008.

[127] L. Cheng, A. K. Agarwal, M. O'Loughin, C. Capell, K. Lam, C. Jonas, J. Richmond, A. Burk, J. W. Palmour, A. A. Ogunniyi, H. K. O'Brien, and C. J. Scozzie, "16 kV, 1 cm^2 4H-SiC PiN diodes for advanced high-power and high-temperature applications," *Materials Science Forum*, vol. 740-742, pp. 895–898, 2013.

[128] M. Snook, H. Hearne, T. McNutt, V. Veliadis, B. Nechay, S. Woodruff, R. S. Howell, D. Giorgi, J. White, and S. Davis, "11.72 cm^2 SiC wafer-scale interconnected 1.8 kV / 64 kA PiN diode," *Materials Science Forum*, vol. 717-720, pp. 961–964, 2012.

[129] "http://www.silvaco.com," January 2013.

[130] U. Lindefelt, "Doping-induced band edge displacements and band gap narrowing in 3C-, 4H-, 6H-SiC and Si," *Journal of Applied Physics*, vol. 84, no. 5, pp. 2628–2637, 1998.

[131] J. Sołtys, J. Piechota, M. Łopuszyński, and S. Krukowski, "A comparative DFT study of electronic properties of 2H-, 4H- and 6H-SiC(0001) and SiC(000$\bar{1}$) clean surfaces: significance of the surface Stark effect," *New Journal of Physics*, vol. 12, p. 043024, 2010.

[132] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proceedings of the IEEE*, vol. 55, no. 12, pp. 2192–2193, 1967.

[133] M. Schadt, G. Pensl, R. P. Devaty, W. J. Choyke, R. Stein, and D. Stephani, "Anisotropy of the electron hall mobility in 4H, 6H, and 15R silicon carbide," *Applied Physics Letters*, vol. 65, no. 24, pp. 3120–3122, December 1994.

[134] W. Shockley and W. T. Read Jr., "Statistics of the recombination of holes and electrons," *Physical Review*, vol. 87, no. 5, pp. 835–842, September 1952.

[135] R. N. Hall, "Electron-hole recombination in germanium," *Physical Review*, vol. 87, p. 387, 1952.

[136] J. G. Fossum and D. S. Lee, "A physical model for the dependence of carrier lifetime on doping density in nondegenerate silicon," *Solid-State Electronics*, vol. 25, no. 8, pp. 741–747, 1982.

[137] S. Selberherr, *Analysis and simulation of semiconductor devices*. Wien, New York: Springer-Verlag, 1984.

[138] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, "Ionization rates and critical fields in 4H silicon carbide," *Applied Physics Letters*, vol. 71, no. 1, pp. 90–92, July 1997.

[139] G. Feng, J. Suda, and T. Kimoto, "Space-modulated junction termination extension for ultrahigh-voltage p-i-n diodes in 4H-SiC," *IEEE Transactions on Electron Devices*, vol. 59, no. 2, pp. 414–418, February 2012.

[140] M. Noborio, J. Suda, and T. Kimoto, "P-channel MOSFETs on 4H-SiC (0001) and nonbasal faces fabricated by oxide deposition and N_2O annealing," *IEEE Transactions on Electron Devices*, vol. 56, no. 9, pp. 1953–1958, 2009.

[141] M. Laube, G. Pensl, and H. Itoh, "Suppressed diffusion of implanted boron in 4H-SiC," *Applied Physics Letters*, vol. 74, no. 16, pp. 2292–2294, 1999.

[142] D. K. Schroder, *Semiconductor Material and Device Characterization - Third Edition*. Hoboken, New Jersey, USA: John Wiley and Sons, 2006.

[143] K. Nakayama, A. Tanaka, M. Nishimura, K. Asano, T. Miyazawa, M. Ito, and H. Tsuchida, "Characteristics of a 4H-SiC PiN diode with carbon implantation/thermal oxidation," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 895–901, April 2012.

[144] P. G. Neudeck, "Perimeter governed minority carrier lifetimes in 4H-SiC p^+n diodes measured by reverse recovery switching transient analysis," *Journal of Electronic Materials*, vol. 27, no. 4, pp. 317–323, 1998.

[145] M. Kato, A. Yoshida, and M. Ichimura, "Estimation of surface recombination velocity from thickness dependence of carrier lifetime in n-type 4H-SiC epilayers," *Japanese Journal of Applied Physics*, vol. 51, p. 02BP12, 2012.

[146] A. Galeckas, J. Linnros, M. Frischholz, and V. Grivickas, "Optical characterization of excess carrier lifetime and surface recombination in 4H/6H-SiC," *Applied Physics Letters*, vol. 79, no. 3, pp. 365–368, 2001.

[147] G. K. Reeves and H. B. Harrison, "Obtaining the specific contact resistance from transmission line model measurements," *IEEE Electron Device Letters*, vol. 3, no. 5, pp. 111–113, May 1982.

[148] E. F. Chor and J. Lerdworatawee, "Quasi-two-dimensional tranmissional line model (QTD-TLM) for planar ohmic contact studies," *IEEE Transactions on Electron Devices*, vol. 49, no. 1, pp. 105–111, January 2002.

[149] "http://cmrf.research.uiowa.edu/scanning-electron-microscopy."

[150] W. L. Bragg, "The diffraction of short electromagnetic waves by a crystal," *Cambridge Philosophical Society*, vol. 17, pp. 43–57, 1914.

[151] "http://www.lsaltd.co.uk/index.html."

[152] "http://www.bath.ac.uk."

[153] H. Harima, "Raman scattering characterisation on 4H-SiC," *Microelectronic Engineering*, vol. 83, pp. 126–129, 2006.

[154] "http://staff.bath.ac.uk/pysdw/newpage11.htm."

[155] W. T. Pike, W. J. Karl, S. Kumar, S. Vijendran, and T. Semple, "Analysis of sidewall quality in through-wafer deep reactive-ion etching," *Microelectronic Engineering*, vol. 73-74, pp. 340–345, 2004.

[156] P. V. Zant, *Microchip Fabrication*. New York, USA: McGraw-Hill, 2004.

[157] F. Lucolano, F. Roccaforte, F. Giannazzo, A. Alberti, and V. Raineri, "Current transport in Ti/Al/Ni/Au ohmic contacts to GaN and AlGaN," *Materials Science Forum*, vol. 556-557, pp. 1027–1030, 2007.

[158] A. Frazzetto, F. Giannazzo, R. L. Nigro, V. Raineri, and F. Roccaforte, "Structural and transport properties in alloyed Ti/Al ohmic contacts formed on p-type Al-

implanted 4H-SiC annealed at high temperature," *Journal of Physics D: Applied Physics*, vol. 44, p. 255302 (9pp), 2011.

[159] "http://www.mathworks.co.uk."

[160] M. Wzorek, A. Czerwinski, A. Kuchuk, J. Ratajczak, A. Piotrowska, and J. Katcki, "TEM characterisation of silicide phase formation in Ni-based ohmic contacts to 4H n-SiC," *Materials Transactions*, vol. 52, no. 3, pp. 315–318, 2011.

[161] J. Crofton, S. E. Mohney, J. R. Williams, and T. Isaacs-Smith, "Finding the optimum Al-Ti alloy composition for use as an ohmic contact to p-type 4H-SiC," *Solid-State Electronics*, vol. 46, no. 1, pp. 109–113, January 2002.

[162] R. Konishi, R. Yasukochi, O. Nakatsuka, Y. Koide, M. Moriyama, and M. Murakami, "Development of Ni/Al and Ni/Ti/Al ohmic contact materials for p-type 4H-SiC," *Materials Science and Engineering: B*, vol. 98, no. 3, pp. 286–293, 2003.

[163] S. Tsukimoto, T. Sakai, and M. Murakami, "Electrical properties and microstructure of ternary Ge/Ti/Al ohmic contacts to p-type 4H-SiC," *Journal of Applied Physics*, vol. 96, no. 9, pp. 4976–4981, November 2004.

[164] L. Kolaklieva, R. Kakanakov, I. Avramova, and T. Marinova, "Nanolayered Au/Ti/Al ohmic contacts to p-type 4H-SiC: Electrical, morphological and chemical performances depending on the chemical composition," *Materials Science Forum*, vol. 556-557, pp. 725–728, 2007.

[165] F. Laariedh, M. Lazar, P. Cremillieu, J. L. Leclercq, and D. Planson, "Investigations on Ni-Ti-Al ohmic contacts obtained on p-type 4H-SiC," *Materials Science Forum*, vol. 711, pp. 169–173, 2012.

[166] "http://www.tanner.com."

[167] "http://www.compugraphics-photomasks.com."

[168] T. Kimoto, N. Inoue, and H. Matsunami, "Nitrogen ion implantation into α-SiC epitaxial layers," *Physica Status Solidi (A)*, vol. 162, no. 1, pp. 263–276, 1997.

[169] A. M. Strel'chuk, E. V. Kalinina, A. A. Lebedev, I. K. Boricheva, and V. V. Pavshukov, "Variant of excess current in 4H-SiC pn structures," in *International Conference on Silicon Carbide and Related Materials (ICSCRM)*, Miyazaki, Japan, October 2013, pp. Tu–P–53.

[170] "http://www.cuttingedgeions.com/home.html," June 2013.

[171] F. Zhao, M. M. Islam, and C.-F. Huang, "Study of sio_2 encapsulation for aluminum and phosphorus implant activation in 4H-SiC," *Materials Letters*, vol. 64, pp. 2593–2596, 2010.

[172] T. Troffer, M. Schadt, T. Frank, H. Itoh, G. Pensl, J. Heindl, H. P. Strunk, and M. Maier, "Doping of SiC by implantation of boron and aluminum," *Physica Status Solidi (A)*, vol. 162, no. 1, pp. 277–298, 1997.

[173] N. E. B. Cowern, K. T. F. Janssen, G. F. A. van de Walle, and D. J. Gravesteijn, "Impurity diffusion via an intermediate species: The B-Si system," *Physical Review Letters*, vol. 65, no. 19, pp. 2434–2437, November 1990.

[174] H. Bracht, N. A. Stolwijk, and M. L. amd G. Pensl, "Diffusion of boron in silicon carbide: Evidence for the kick-out mechanism," *Applied Physics Letters*, vol. 77, no. 20, pp. 3188–3190, 2000.

[175] "http://gwyddion.net."

[176] "http://www.bigfreshcontrol.com/documents/act_documents/silica_fume_msds.pdf."

[177] H. Kurimoto, K. Shibata, C. Kimura, H. Aoki, and T. Sugino, "Thermal oxidation temperature dependence of 4H-SiC MOS interface," *Applied Surface Science*, vol. 253, pp. 2416–2420, 2006.

[178] Y. Hijikata, H. Yaguchi, and S. Yoshida, "A kinetic model of silicon carbide oxidation based on the interfacial silicon and carbon emission phenomenon," *Applied Physics Express*, vol. 2, p. 021203, 2009.

[179] K. Kawahara, J. Suda, and T. Kimoto, "Analytical model for reduction of deep levels in SiC by thermal oxidation," *Journal of Applied Physics*, vol. 111, p. 053710, 2012.

[180] V. V. Evstrapov, K. V. Kiselev, I. L. Petrovich, and B. V. Tsarenkov, "Current due to recombination via multilevel centers in space charge layer of p-n structure," *Soviet Physics Semiconductors*, vol. 18, no. 10, pp. 1156–1159, 1984.

[181] "http://www.abb.co.uk."